

## PATENT ABSTRACTS OF JAPAN

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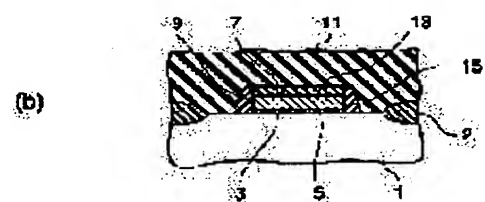
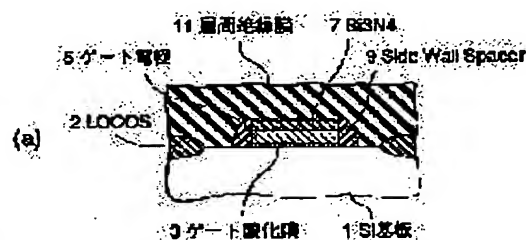
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## (54) SEMICONDUCTOR DEVICE AND FABRICATION THEREOF

(57)Abstract:

**PROBLEM TO BE SOLVED:** To provide a semiconductor device, and a fabrication method thereof, in which variation of the threshold voltage is suppressed by reducing the fluctuations in the work function of a finished gate electrode caused by the hot process which may be included in the fabrication process subsequent to formation of the gate electrode.

**SOLUTION:** A gate oxide 3 is deposited on the surface of a silicon substrate 1 and a gate electrode 5 is formed thereon. The gate electrode 5 is formed of a thin p<sup>+</sup>-type poly-Si film doped with B. Si<sub>3</sub>N<sub>4</sub> 7 is deposited on the gate electrode 5 and a Side Wall Spacer 9 is formed of Si<sub>3</sub>N<sub>4</sub> film on the side wall of the gate electrode 5. An interlayer insulator 11 of SiO<sub>2</sub> is deposited on the Si<sub>3</sub>N<sub>4</sub> 7, the Side Wall Spacer 9 and an LOCOS oxide 2. According to the structure, diffusion of B from the gate electrode 5 into the interlayer insulator 11 can be suppressed during hot process after formation of the gate electrode 5.



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CLAIMS

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[Claim(s)]

[Claim 1] it was formed on the gate electrode which was formed through gate dielectric film on the semiconductor substrate and which introduced the high-concentration impurity, the insulator layer or electric conduction film containing the nitrogen formed in the upper part and the side-attachment-wall section of this gate electrode, and this insulator layer or the electric conduction film -- at least -- SiO<sub>2</sub> Semiconductor device characterized by providing the included interlayer insulation film.

[Claim 2] the above-mentioned gate electrode -- p+Poly Si from -- semiconductor device according to claim 1 characterized by becoming.

[Claim 3] The above-mentioned gate electrode is WSix. Poly Si Semiconductor device according to claim 1 characterized by consisting of Polycide of two-layer structure.

[Claim 4] The semiconductor device according to claim 1 characterized by the above-mentioned gate electrode consisting of a silicide monolayer.

[Claim 5] The semiconductor device according to claim 1 characterized by the above-mentioned impurity being B.

[Claim 6] Si<sub>3</sub> N<sub>4</sub> which the insulator layer containing the above-mentioned nitrogen deposited by LP-CVD or Plasma CVD Semiconductor device according to claim 1 characterized by being the film or the SiON film.

[Claim 7] Si<sub>3</sub> N<sub>4</sub> which the insulator layer containing the above-mentioned nitrogen deposited by LP-CVD or Plasma CVD The film or the SiON film, and SiO<sub>2</sub> Semiconductor device according to claim 1 characterized by being the insulator layer of two-layer structure with the film.

[Claim 8] The semiconductor device according to claim 1 characterized by being the nitriding oxide film with which the above-mentioned gate dielectric film comes to nitride an oxide film.

[Claim 9] The process which forms gate dielectric film on a semi-conductor substrate, and the process which deposits the electric conduction film on this gate dielectric film, The process which introduces an impurity into this electric conduction film, the process which deposits the insulator layer containing nitrogen on this electric conduction film, and by processing this insulator layer and the electric conduction film the process which leaves an insulator layer on the gate electrode which consists of this electric conduction film, the process which forms the insulator layer which contains nitrogen in the side attachment wall of this insulator layer and this gate electrode, and this insulator layer top -- SiO<sub>2</sub> from -- the manufacture approach of the semiconductor device characterized by providing the process which deposits the becoming interlayer insulation film.

[Claim 10] The manufacture approach of the semiconductor device according to claim 9 characterized by the above-mentioned impurity being B.

[Claim 11] the above-mentioned electric conduction film -- p+Poly Si from -- the manufacture approach of the semiconductor device according to claim 9 characterized by becoming.

[Claim 12] Si<sub>3</sub> N<sub>4</sub> which the insulator layer containing the above-mentioned nitrogen deposited by LP-CVD or Plasma CVD The manufacture approach of the semiconductor device according to claim 9 characterized by being the film or the SiON film.

[Claim 13] Si<sub>3</sub> N<sub>4</sub> which the insulator layer containing the above-mentioned nitrogen deposited by LP-CVD or Plasma CVD The film or the SiON film, and SiO<sub>2</sub> The manufacture approach of the semiconductor device according to claim 9 characterized by being the insulator layer of two-layer structure with the film.

[Claim 14] The manufacture approach of the semiconductor device characterized by providing the process which forms gate dielectric film on a semi-conductor substrate, the process which deposits the refractory metal silicide film on this gate dielectric film, the process which forms the thin film for out-diffusion prevention of an impurity

on this refractory metal silicide film, and the process which introduces an impurity into this refractory metal silicide film through this thin film.

[Claim 15] The manufacture approach of the semiconductor device characterized by to provide the process which forms gate dielectric film on a semi-conductor substrate, the process which deposits the refractory metal silicide film on this gate dielectric film, the process which carries out pattern NINGU of this refractory metal silicide film, and forms a gate electrode, the process which forms the thin film for out-diffusion prevention of an impurity in all or some of these gate electrode surfaces, and the process which introduce an impurity into this gate electrode through this thin film.

[Claim 16] The thin film for the above-mentioned out-diffusion prevention is LP. - Si<sub>3</sub>N<sub>4</sub> formed by the CVD method The manufacture approach of the semiconductor device according to claim 14 or 15 characterized by being the film.

[Claim 17] The manufacture approach of the semiconductor device according to claim 14 or 15 characterized by the thin film for the above-mentioned out-diffusion prevention being the metal nitride formed by nitriding this refractory metal silicide film directly.

[Claim 18] The above-mentioned refractory metal silicide film is WSix. The film or MoSix The manufacture approach of the semiconductor device according to claim 14 or 15 characterized by being the film.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a semiconductor device and its manufacture approach. It is related with the semiconductor device which can maintain the property stabilized also after the semiconductor device which has the gate electrode with which B (boron) was doped especially went through the subsequent thermal process, and its manufacture approach. Moreover, it is related with the manufacture approach of a semiconductor device of having the refractory metal gate electrode with which the work function was controlled by the class of impurity introduced, and its concentration.

[0002]

[Description of the Prior Art] It is known by using SOI (Silicon on Insulator) structure that full separation between components becomes easy and that control of a latch rise peculiar to a soft error or CMOS<sub>Tr</sub> will be attained. Moreover, examination about what the high speed and high-reliability-ization of CMOS<sub>Tr</sub> LSI are attained for using the SOI structure where the thickness of Si barrier layer is about 500nm has been performed comparatively early.

[0003] Recently, it has turned out that make Si layer on the front face of SOI thin to about 100 morenm, and it controls in the condition that the high impurity concentration of a channel is also comparatively low, and the further excellent engine performance, such as control of a short channel effect and improvement in the current drive capacity of MOS<sub>Tr</sub>, will be obtained if it is made conditions (perfect depletion mold) which the whole Si barrier layer depletion-izes mostly.

[0004] However, n+Poly Si used abundantly from the former When using as gate electrode material to NMOS<sub>Tr</sub>, in order to carry out the threshold electrical potential difference  $V_{th}$  near [ 0.5 - 1.0V ] <sub>Tr</sub> usual enhancement type, it is -1017-/cm<sup>2</sup> about the high impurity concentration of a channel. It must carry out above. Then, in order to produce enhancement type <sub>Tr</sub> with a perfect depletion mold, examination which uses p+Poly Si (B-DOPOS) as a gate ingredient is performed in recent years.

[0005] Bulk Si to which detailed-ization progresses on the other hand It also sets to a device and is Poly Si of the above-mentioned n mold. N channel, NMOS<sub>Tr</sub> is received for the purpose of also using the work function of a gate electrode and adjusting  $V_{th}$ , since a P channel cannot form MOS<sub>Tr</sub> of a surface channel mold strong against a short channel effect in coincidence. To n+Poly Si and PMOS<sub>Tr</sub>, it is p+Poly Si. Dual Gate used, respectively A process is examined and it is for the first time.

[0006] Drawing 33 (a) is the expanded sectional view showing the gate electrode in the semiconductor device which is the sectional view showing the conventional semiconductor device, and shows drawing 33 (b) to drawing 33 (a), and its near part (field of A), and is p+Poly Si. After forming a gate electrode, the trouble produced by giving a heat treatment process is shown.

[0007] As shown in drawing 33 (a), the LOCOS oxide film 103 for performing isolation is formed in the front face of a silicon substrate 101. next, p+Poly Si which doped B through gate oxide 102 on the silicon substrate 101 (Dope) from -- the becoming gate electrode 105 forms -- having -- a this gate electrode 105 and silicon substrate 101 top -- SiO<sub>2</sub> from -- the becoming interlayer insulation film 107 is formed.

[0008]

[Problem(s) to be Solved by the Invention] By the way, p+Poly Si which doped this B (Dope) When it uses as a gate electrode 105, depending on the thermal process after doping B to the gate electrode 105 SiO<sub>2</sub> whose B in the gate electrode 105 is an interlayer insulation film 107 as shown in drawing 33 (b) etc. -- a deposit (deposit 111 of B) -- carrying out -- and B -- comparatively -- quick -- SiO<sub>2</sub> Inside is diffused (diffusion 113 to the

interlayer insulation film of B). For this reason, Poly Si The concentration of inner B falls and it is Poly Si. In depletion-izing \*\*\*\*, it is p+Poly Si by this. A work function will be changed. in addition, same SiO<sub>2</sub> it is -- even if -- it is enlarged [ the diffusion coefficient of B ] by the inside of the interlayer insulation film 107 which is inferior to compactness from gate oxide 102.

[0009] That is, since the degree of the diffusion 113 to the interlayer insulation film of B changes according to the temperature of a next thermal process consequently, variation arises also in change of the work function of the gate electrode 105. Therefore, this p+Poly Si The variation in each property which makes the start V<sub>th</sub> variation of the transistor used for the gate electrode 105 will increase.

[0010] Moreover, variation in each above property and p+Poly Si It is becoming still more difficult to form the component of the property which lessened the field internal division cloth of the work function of the gate, and was stabilized in respect of the following. p+Poly Si of the completion by fluctuation of the thermal process after introducing an impurity into a gate electrode p+Poly Si by difference of the thermal process at the time of manufacture by the difference between fluctuation of the property of a gate electrode and the type of a semiconductor device It is because the effectual temperature distribution within a Wafer side also increase by diameter-ization of macrostomia of not only fluctuation of a work function but the adoption of RTA (Rapid Thermal Anneal) with temperature distribution large especially in recent years and Wafer etc.

[0011] Consequently, this p+Poly Si V<sub>th</sub> of Tr which used this for the gate electrode corresponding to fluctuation of a work function will be changed in a field, and is becoming a big trouble on semiconductor device production for future low-battery-izing and low-power-izing. that is, -- if p+Poly Si (B-DOPOS) is used as a gate ingredient -- Channel -- Non-Dope it is -- V<sub>th</sub> is set a little to -1V to slight height by the case, and it is becoming a problem in the future device with which supply voltage falls for low-power-izing.

[0012] Moreover, the above troubles are p+Poly Si by which B was doped. Not only when it is the gate electrode of a monolayer, but SiO<sub>2</sub> W-Polycide which is the problem generally observed when using the gate electrode with which B which is an impurity with an inner large diffusion coefficient was doped for example, by which B was doped WSix by which the gate and B were doped The case of the monolayer gate etc. is also a common problem. That is, it is Doping to refractory metal silicide about an impurity like B. Since the diffusion coefficient of B in SiO<sub>2</sub> which are silicide and the insulator layer which usually encloses a gate electrode is very large when it carries out, even if it introduces B of a certain constant rate, B concentration in the silicide of completion will be changed according to a subsequent thermal process. Consequently, WSix of completion It is Dose of B about the work function of the gate. It was impossible to have controlled only by the amount to the work function made into an aim.

[0013] Moreover, WSix Examination which uses refractory metal silicide [ like ] by the monolayer, and adjusts V<sub>th</sub> of SOITr of a perfect depletion mold to a suitable value is also beginning to be performed. As for refractory metal silicide like WSix, generally, there is much what has the work function near [ Mid-Gap ] Si. the case where refractory metal silicide is used for the gate electrode of SOITr of a perfect depletion mold -- V<sub>th</sub> -- Channel -- Non-Dope it is -- it becomes --0.5V and a suitable value by -0.5V and P-MOS by N-MOS at the time.

[0014] furthermore, WSix MoSix refractory metal silicide [ like ] -- a gate electrode -- using -- the presentation -- a stoichiometric composition ratio -- Si Rich \*\* -- introducing B, when it carries out -- Non-Dope comparing and introducing As to the p+Si side -- Non-Dope It has become clear that it compares and some of the work function can be adjusted to the n+Si side.

[0015] Moreover, about the V<sub>th</sub> control of Tr by the impurity of Channel, the problem of increase of V<sub>th</sub> dispersion by statistical fluctuation is pointed out from detailed-izing of Tr size, and reduction of the amount of impurities contained in the Channel section of Tr per [ in accordance with it ] piece. Although this is not the demand which approached like [ in SOITr of a perfect depletion mold ], it is a technique which can creep in the future and is needed.

[0016] As mentioned above, controlling correctly to the value of V<sub>th</sub> with an eye on the semiconductor device which has Tr of V<sub>th</sub> which has good control of striking the class of impurity and its concentration in any direction according to various kinds of Tr(s) by the ion implantation, and is different from a situation which was described when manufacturing the semiconductor device which has the refractory metal silicide gate electrode by which the work function was controlled is called for. That is, the manufacture approach of a suitable semiconductor device of not fluctuating Profile of the impurity in the gate electrode after an ion implantation is searched for.

[0017] The purpose of invention which this invention is made in consideration of the above situations, and relates to claims 1-13 is to offer the semiconductor device which suppressed fluctuation of the work function of the gate electrode of the completion produced according to that thermal process, and made small variation in a

threshold electrical potential difference, and its manufacture approach, even when a thermal process is in the production process after forming the gate electrode which introduced the high-concentration impurity.

[0018] Moreover, the purpose of invention concerning claims 14-18 is also in the process which forms a diffusion barrier layer at an elevated temperature comparatively to offer the manufacture approach of a semiconductor device correctly controllable to the value with an eye on the high impurity concentration of a gate electrode, in order to control the out-diffusion of the impurity in a gate electrode.

[0019]

[Means for Solving the Problem] the semiconductor device concerning this invention was formed on the gate electrode which was formed through gate dielectric film on the semi-conductor substrate and which introduced the high-concentration impurity, the insulator layer or the electric conduction film containing the nitrogen formed in the upper part and the side attachment wall section of this gate electrode, and this insulator layer or the electric conduction film in order to solve the above-mentioned technical problem -- at least --  $\text{SiO}_2$  it is characterize by to provide the include interlayer insulation film.

[0020] Moreover, the manufacture approach of the semiconductor device concerning this invention The process which forms gate dielectric film on a semi-conductor substrate, and the process which deposits the electric conduction film on this gate dielectric film, The process which introduces an impurity into this electric conduction film, the process which deposits the insulator layer containing nitrogen on this electric conduction film, and by processing this insulator layer and the electric conduction film the process which leaves an insulator layer on the gate electrode which consists of this electric conduction film, the process which forms the insulator layer which contains nitrogen in the side attachment wall of this insulator layer and this gate electrode, and this insulator layer top --  $\text{SiO}_2$  from -- it is characterized by providing the process which deposits the becoming interlayer insulation film.

[0021] By the above-mentioned semiconductor device and its manufacture approach, the insulator layer containing nitrogen is formed on the gate electrode which introduced the high-concentration impurity, and the insulator layer which contains nitrogen in the side attachment wall of a gate electrode is formed. For this reason, even if a thermal process is in the production process after forming a gate electrode, the impurity in a gate electrode is  $\text{SiO}_2$  in that case. It can control being spread in the direction of the included interlayer insulation film. Therefore, the impurity introduced into the gate electrode can be activated effectively, fluctuation by the thermal process of the work function of the gate electrode of completion is suppressed, and variation in a threshold electrical potential difference can be made small.

[0022] Moreover, the manufacture approach of the semiconductor device concerning this invention is characterized by providing the process which forms gate dielectric film on a semi-conductor substrate, the process which deposits the refractory metal silicide film on this gate dielectric film, the process which forms the thin film for out-diffusion prevention of an impurity on this refractory metal silicide film, and the process which introduces an impurity into this refractory metal silicide film through this thin film.

[0023] By the manufacture approach of the above-mentioned semiconductor device, after forming the thin film for out-diffusion prevention of an impurity on the refractory metal silicide film, the impurity is introduced into the refractory metal silicide film through this thin film. The problem produced when an impurity is introduced into the refractory metal silicide film (gate electrode) by this before forming the thin film for out-diffusion prevention as a diffusion barrier layer of an impurity is lost. That is, it is because the spatial redistribution of the out-diffusion of the impurity in the refractory metal silicide film by the thermal process at the time of formation of this thin film or a longitudinal direction can be controlled.

[0024] Moreover, the manufacture approach of the semiconductor device concerning this invention The process which forms gate dielectric film on a semi-conductor substrate, and the process which deposits the refractory metal silicide film on this gate dielectric film, It is characterized by providing the process which carries out pattern NINGU of this refractory metal silicide film, and forms a gate electrode, the process which forms the thin film for out-diffusion prevention of an impurity in all or some of these gate electrode surfaces, and the process which introduces an impurity into this gate electrode through this thin film.

[0025] By the manufacture approach of the above-mentioned semiconductor device, after carrying out pattern NINGU of the refractory metal silicide film, the thin film for out-diffusion prevention of an impurity is formed in all or some of gate electrode surfaces, and an impurity is introduced into this gate electrode through this thin film after that. Thereby, the work function of a gate electrode is decided according to high impurity concentration with one simple substance Tr, and fluctuation of the work function by the counter diffusion of the longitudinal direction of the impurity in a gate electrode is not produced.

[0026]

[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained with reference to a drawing. Drawing 1 (a) is the sectional view showing the semiconductor device by the gestalt of implementation of the 1st of this invention. p+Poly Si by which B (boron) for which this semiconductor device is used with a semiconductor integrated circuit was doped from -- it has the becoming gate electrode.

[0027] It is Bulk as shown in drawing 1 (a). The LOCOS oxide film 2 is formed in the front face of a silicon substrate 1. Gate oxide 3 is formed on the front face of the silicon substrate 1 between this LOCOS oxide-film 2, and the gate electrode 5 is formed on this gate oxide 3. This gate electrode 5 is Poly Si whose thickness is 150nm. It is formed with the film and is this Poly Si. It is doped in it in the amount of dose (Dose) whose B is about  $[5 \times 10^{15} \text{cm}^{-2}]$  two, and the film is p+. It is a mold. In addition, this Poly Si B concentration in the film is  $-3.3 \times 10^{20} \text{cm}^{-3}$ .

[0028] Si<sub>3</sub>N<sub>4</sub> whose thickness is about 150nm on the gate electrode 5 The film 7 is formed and it is Spacer in the side attachment wall of the gate electrode 5. Si<sub>3</sub>N<sub>4</sub> whose width of face is about 150nm Side Wall Spacer 9 which consists of film is formed. in addition, Si<sub>3</sub>N<sub>4</sub> the film 7 and Side Wall Spacer 9 -- LPCVD (Low Pressure Chemical Vapor Deposition) -- it is formed of law.

[0029] Si<sub>3</sub>N<sub>4</sub> the film 7, Side Wall Spacer 9, and LOCOS oxide-film 2 top -- SiO<sub>2</sub> from -- the becoming interlayer insulation film 11 is formed.

[0030] According to the gestalt of implementation of the above 1st, it is Si<sub>3</sub>N<sub>4</sub> on the gate electrode 5. The film 7 is formed and it is Si<sub>3</sub>N<sub>4</sub> to the side attachment wall of the gate electrode 5. Side Wall Spacer 9 which consists of film is formed. For this reason, even if a thermal process is in the production process after forming the gate electrode 5, it can control that B in the gate electrode 5 is spread in the direction of an interlayer insulation film (SiO<sub>2</sub>) 11 in that case (out-diffusion). Therefore, B doped to the gate electrode 5 can be activated effectively, the fluctuation (heterogeneity of a work function) by the thermal process of the work function of the gate electrode 5 of completion is suppressed, and variation in a threshold electrical potential difference can be made small.

[0031] Moreover, p+Poly Si of the work function stabilized since it was hard to be influenced of the thermal process after gate electrode 5 formation It becomes possible to form a gate electrode. Therefore, although the thermal processes given to it will also differ if the classes of semiconductor device to manufacture differ, the thermal process is embraced even in such a case, and it is p+Poly Si of completion. It can lose changing the work function of a gate electrode. Furthermore, even when the effectual temperature distribution within a Wafer side increase by large adoption of temperature distribution of RTA, diameter-ization of macrostomia of Wafer, etc., it is p+Poly Si of completion. The component of the property which lessened the field internal division cloth of the work function of a gate electrode, and was stabilized can be formed.

[0032] In addition, Poly Si by which B was doped with the gestalt of implementation of the above 1st WSix by which B was doped although the gate electrode 5 of a monolayer was used Poly Si WSix which is possible also for using the gate electrode of Polycide of two-layer structure and by which B was doped It is also possible to use the gate electrode of a silicide monolayer [ like ].

[0033] Moreover, although B concentration in the gate electrode 5 is set to  $-3.3 \times 10^{20} \text{cm}^{-3}$ , it is also possible for it not to be limited to this but to choose B concentration according to each device.

[0034] Moreover, Si<sub>3</sub>N<sub>4</sub> formed of LP-CVD as film which controls diffusion of B from the gate electrode 5 It is also possible to use an insulator layer like [ although film 7 and 9 is used ] the SiON film formed of Plasma CVD as film which controls diffusion of B from the gate electrode 5, and it is also possible to use conductive film like TiN formed by CVD or the Sputter method.

[0035] Moreover, although B within a solid-solution limit is doped to the gate electrode 5, it is also possible to dope sufficient B which exceeds a solid-solution limit to the gate electrode 5. Thus, when doping B exceeding a solid-solution limit and heat-treating to a silicon substrate (Wafer) for activating B in a gate electrode, even if there are temperature distribution of extent which is in a Wafer side, it is absorbed, and properties, such as a work function of each gate electrode of completion, are not changed, namely, the property of each gate electrode can be stabilized.

[0036] Moreover, it is Si<sub>3</sub>N<sub>4</sub> to the upper part and the side-attachment-wall section of the gate electrode 5. Although film 7 and 9 is formed, it is also possible to form the electric conduction film which contains nitrogen in the upper part and the side-attachment-wall section of the gate electrode 5.

[0037] Drawing 1 (b) is the sectional view of the semiconductor device in which the modification of the semiconductor device by the gestalt of the 1st operation shown in drawing 1 (a) is shown, gives the same sign to

the same part as drawing 1 (a), and explains only a different part.

[0038] Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm on the gate electrode 5 Si<sub>3</sub>N<sub>4</sub> whose thickness the film 7 is formed and is about -10nm at the side attachment wall of the gate electrode 5 The film 9 is formed. Si<sub>3</sub>N<sub>4</sub> On the film 7, it is SiO<sub>2</sub>. The film 13 is formed and it is Si<sub>3</sub>N<sub>4</sub>. In the side face of the film 9, it is SiO<sub>2</sub>. The film 15 is formed. moreover, Si<sub>3</sub>N<sub>4</sub> SiH<sub>2</sub> Cl<sub>2</sub> usual in film 7 and 9 NH<sub>3</sub> LPCVD by the thermal reaction of mixed gas -- it is formed of law. In addition, it is the insulator layer and Spacer of OffSet of the upper part of the gate electrode 5, and the side-attachment-wall section in this way. They are SiO<sub>2</sub> / Si<sub>3</sub>N<sub>4</sub> as an insulator layer. It is the insulator layer and Spacer of OffSet to use the two-layer film. It is for considering as the value of a request of width of face.

[0039] Also in the above-mentioned modification, the same effectiveness as the gestalt of the 1st operation can be acquired.

[0040] moreover -- above -- Si<sub>3</sub>N<sub>4</sub> of the upper part of the gate electrode 5, and the side-attachment-wall section although thickness of film 7 and 9 is thin-film-ized to about -10nm -- usual SiH<sub>2</sub> Cl<sub>2</sub> NH<sub>3</sub> LPCVD by the thermal reaction of mixed gas -- Si<sub>3</sub>N<sub>4</sub> formed by law the film -- even if it is several nm thickness, it fully has the barrier property to diffusion of impurities, such as B.

[0041] Moreover, Si<sub>3</sub>N<sub>4</sub> The increment in the dielectric constant of an interlayer film can be suppressed by forming the thickness of film 7 and 9 thinly with about -10nm. For this reason, while being able to operate a semiconductor device more at high speed, it is high LP-Si<sub>3</sub>N<sub>4</sub> of stress. The fall of the dependability of the device by the film can be suppressed to the minimum. However, when using film like SiON by which stress and a presentation were controlled using Plasma CVD etc., even if it forms the SiON film comparatively thickly, the increment in stress or a dielectric constant can be disregarded.

[0042] Drawing 2 - drawing 11 are the sectional views showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and also show the production process for producing the structure of the gate electrode shown in drawing 1 (a).

[0043] First, as shown in drawing 2, the LOCOS oxide film 2 and Well which is not illustrated are prepared in a silicon substrate 1, and isolation is performed using this LOCOS oxide film 2, Well, etc. Next, on the front face of the silicon substrate 1 of a component field, gate oxide 3 is formed by the oxidizing [ thermally ] method (growth).

[0044] Then, Poly Si whose thickness it is thin to a gate electrode on gate oxide 3 and the LOCOS oxide film 2 is about -150nm as shown in drawing 3 The film 5 accumulates.

[0045] Next, it is Poly Si as shown in drawing 4. The photoresist film 21 is formed on the film 5. The pattern configuration of this photoresist film 21 carries out opening of the P-MOS section. Then, it is Poly Si, using this photoresist film 21 as a mask. B is doped by the film 5 by the ion implantation 23 of BF<sub>2</sub><sup>+</sup>.

[0046] In addition, in order to consider as the device of the surface channel mold with which the fall of the threshold electrical potential difference V<sub>th</sub> by the short channel effect cannot produce both N-MOSTr and P-MOSTr easily, it is n<sup>+</sup> to N-MOS. It is p<sup>+</sup> to the gate and P-MOS. It is necessary to adopt the gate, respectively. Therefore, the ion implantation to the gate is had good control of striking in any direction with a resist mask.

[0047] Then, as shown in drawing 5, the above-mentioned photoresist film 21 is removed, and it is p<sup>+</sup>PolySi. On the film 5, Si<sub>3</sub>N<sub>4</sub> film 7 whose thickness is about -150nm accumulates by the LPCVD method. Si<sub>3</sub>N<sub>4</sub> at this time For example, using a vertical mold CVD system, temperature is set into 760 degrees C, they set a pressure to 53Pa, and the deposition conditions of the film 7 are SiH<sub>2</sub> Cl<sub>2</sub> / NH<sub>3</sub> / N<sub>2</sub>. It considers as the flow rate of 90/600/500sccm using reactant gas, respectively.

[0048] Next, as shown in drawing 6, it is Si<sub>3</sub>N<sub>4</sub>. The photoresist film 25 is formed on the film 7, and this photoresist film 25 has the pattern of a gate electrode.

[0049] Then, it is Si<sub>3</sub>N<sub>4</sub>, using this photoresist film 25 as a mask, as shown in drawing 7. Etching processing of the film 7 is carried out. Si<sub>3</sub>N<sub>4</sub> at this time The processing conditions of the film 7 are for example, the magnetron mold Etcher. It uses, and temperature is set into 20 degrees C, a pressure is set to 2.7Pa, and they are 1000W and CHF<sub>3</sub> about RFPower. A flow rate is set to 45sccm(s). Next, the photoresist film 25 is removed.

[0050] Next, as shown in drawing 8, it is Si<sub>3</sub>N<sub>4</sub>. It is p<sup>+</sup>Poly Si, using the film 7 as a mask. Etching processing of the film 5 is carried out. Thereby, gate oxide 3 is minded on a silicon substrate 1, and it is p<sup>+</sup>Poly Si. The gate electrode 5 which consists of film is formed. Then, the LDD layer which is not illustrated is formed in a silicon substrate 1 by introducing an impurity into the LDD field in a silicon substrate 1 which is not illustrated (ion implantation). In addition, an ion implantation is with the case of N-MOSTr, and the case of P-MOSTr, that is, the case of an N channel, and in the case of a P channel, it is necessary to have good control of striking it in any

direction suitably using a resist mask.

[0051] Then, as shown in drawing 9, in the whole surface, it is Si<sub>3</sub>N<sub>4</sub>. The film accumulates. Next, this Si<sub>3</sub>N<sub>4</sub> Etch Back [ film ] using anisotropy processing By carrying out, it is Si<sub>3</sub>N<sub>4</sub> in the side attachment wall of the gate electrode 5. LDD which consists of film Spacer 9 is formed. Si<sub>3</sub>N<sub>4</sub> at this time Both membranous deposition conditions and processing conditions use the above-mentioned thing.

[0052] Next, after depositing the thin oxide film for channeling prevention which is not illustrated, as shown in drawing 10, the photoresist film 27 is formed on a silicon substrate 1. The pattern configuration of this photoresist film 27 carries out opening of the source drain field formation section. Then, the diffusion layer of the source drain field which is not illustrated is formed by carrying out the installation 29 of an impurity, for example, the ion implantation of BF<sub>2</sub><sup>+</sup>, to a silicon substrate 1 by using this photoresist film 27 as a mask. In addition, this ion implantation is with the case of N-MOSTr, and the case of P-MOSTr, that is, the case of an N channel, and in the case of a P channel, it is necessary to have good control of striking it in any direction suitably using a resist mask.

[0053] Next, after removing the photoresist film 27, heat treatment (annealing) for activating the gate electrode 5, a LDD layer, the diffusion layer of a source drain field, and other impurity installation layers is performed. For example, in Ar ambient atmosphere, temperature is made into 1000 degrees C, they make the processing time 10 seconds, and RTA processing is used for the heat treatment conditions at this time.

[0054] Then, as shown in drawing 11, it is Si<sub>3</sub>N<sub>4</sub> in the usual process. The film 7, SideWall An interlayer insulation film 11 accumulates on Spacer 9 and a silicon substrate 1. Next, contact hole 11a is prepared in this interlayer insulation film 11, a gap is filled by metal 31, wiring 33 is formed on this metal 31, and the inside of this contact hole 11a completes a component.

[0055] According to the gestalt of implementation of the above 2nd, it is Si<sub>3</sub>N<sub>4</sub> on the gate electrode 5. The film 7 is formed and it is Si<sub>3</sub>N<sub>4</sub> to the side attachment wall of the gate electrode 5. Side Wall Spacer 9 which consists of film is formed. For this reason, it can control that B in the gate electrode 5 is spread in the direction of an interlayer insulation film (SiO<sub>2</sub>) 11 in the case of the thermal process after forming the gate electrode 5 (out-diffusion). Therefore, B doped to the gate electrode 5 can be activated effectively, fluctuation by the thermal process of the work function of the gate electrode 5 of completion is suppressed, and variation in a threshold electrical potential difference can be made small.

[0056] moreover, p+Poly Si of the work function stabilized since it was hard to be influenced of the thermal process after gate electrode 5 formation from -- it becomes possible to form the becoming gate electrode 5. Therefore, although the thermal processes given to it will also differ if the classes of semiconductor device to manufacture differ, the thermal process is embraced even in such a case, and it is p+PolySi of completion. It can lose changing the work function of a gate electrode. Furthermore, even when the effectual temperature distribution within a Wafer side increase by large adoption of temperature distribution of RTA, diameter-ization of macrostomia of Wafer, etc., it is p+Poly Si of completion. The component of the property which lessened the field internal division cloth of the work function of a gate electrode, and was stabilized can be formed.

[0057] That is, it is Si<sub>3</sub>N<sub>4</sub> about a gate electrode. By surrounding by the insulator layer which controls diffusion of an impurity [ like ], it can prevent B in the gate electrode 5 after heat treatment decreasing by out-diffusion. That is, it is not concerned with the existence of heat treatment after gate electrode 5 formation, the height of heat treatment temperature, and the merits and demerits of heat treatment time amount, but B concentration in the gate electrode 5 can be maintained while it has been [ at the time of B dope ] high. For this reason, even if this thermal process changes or the effectual temperature distribution within the Wafer side in a thermal process get worse, fluctuation of B concentration in the gate electrode of completion can be made small.

[0058] In addition, Poly Si by which B was doped with the gestalt of implementation of the above 2nd It is WSix although the manufacture approach of the semiconductor device using the gate electrode 5 of a monolayer is explained. The thing using the gate electrode of Polycide of two-layer structure with Poly Si may be used, and it is WSix. The thing using the gate electrode of a silicide monolayer [ like ] may be used.

[0059] Moreover, although the device about Tr formed on the Bulk Si substrate 1 is used, it is also possible to use the device of SOI structure.

[0060] Moreover, it is Si<sub>3</sub>N<sub>4</sub> as an insulator layer for diffusion prevention. The film 7 and LDD Although the manufacture approach of the semiconductor device using Spacer 9 is explained For example, thin LP-Si<sub>3</sub>N<sub>4</sub> The film and SiO<sub>2</sub> If it combines and deposits with SiO<sub>2</sub> / Si<sub>3</sub>N<sub>4</sub> = 140 / 10nm The rest is the OffSet insulator layer and Side Wall Spacer of the gate. It is also possible to produce the semiconductor device shown in drawing 1 (b) only by changing some membranous processing conditions.

[0061] namely, Poly Si shown in drawing 5 a film 5 top -- LPCVD -- Si<sub>3</sub>N<sub>4</sub> whose thickness is about -150nm by law After depositing the film 7 As shown in drawing 9 , it is Si<sub>3</sub>N<sub>4</sub> to the whole surface. The film is deposited and it is this Si<sub>3</sub>N<sub>4</sub>. Etch Back [ film ] using anisotropy processing By carrying out, it is Si<sub>3</sub>N<sub>4</sub> to the side attachment wall of the gate electrode 5. LDD which consists of film Although Spacer 9 is formed Poly Si a film 5 top -- LPCVD -- thin Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm by law The film is deposited. This Si<sub>3</sub>N<sub>4</sub> SiO<sub>2</sub> whose thickness is about -140nm on the film After depositing the film, the side attachment wall of the gate electrode 5 -- LPCVD -- thin Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm by law the film -- forming -- further -- this Si<sub>3</sub>N<sub>4</sub> SiO<sub>2</sub> whose thickness is about -140nm at a membranous side attachment wall By forming the film It is Si<sub>3</sub>N<sub>4</sub> to the side attachment wall of the gate electrode 5. The film and SiO<sub>2</sub> LDD which consists of film Spacer Forming is also possible. moreover, LPCVD usual as mentioned above -- Si<sub>3</sub>N<sub>4</sub> formed by law if it is the film - the out-diffusion of impurities, such as B from a gate electrode, can fully be controlled by thickness (several nm or -10nm).

[0062] Moreover, although gate oxide 3 is formed by the oxidizing [ thermally ] method on the front face of a silicon substrate 1, it is also possible to form the gate dielectric film which consists of a nitriding oxide film which comes to nitride an oxide film on the front face of a silicon substrate 1. That is, although what is necessary is just to control the out-diffusion in the upper part and the side-attachment-wall section of the gate electrode 5 since B concentration in the gate electrode 5 falls by carrying out out-diffusion of the B doped by the gate electrode 5 through the interlayer insulation film 11 with a mainly large diffusion coefficient Preferably, in order to control the diffusion rate of B also about gate oxide 3, it is good to adopt the nitriding oxide film which comes to nitride an oxide film 3, to control further the fall of B concentration in the gate electrode 5, and to fully control fluctuation of the work function of the gate electrode 5 of completion etc.

[0063] It is WSix by which drawing 12 - drawing 22 are the sectional views showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and the work function with which the gestalt of this operation was formed on the Bulk Si substrate in this invention was controlled. It applies to manufacture of the MOS mold semiconductor device which has a gate electrode.

[0064] First, as shown in drawing 12 , the LOCOS oxide film 2 and Well which is not illustrated are prepared in a silicon substrate 1, and isolation is performed using this LOCOS oxide film 2, Well, etc. Next, on the front face of the silicon substrate 1 of a component field, gate oxide 3 is formed by the oxidizing [ thermally ] method (growth).

[0065] Then, WSix whose thickness it is thin to a gate electrode on gate oxide 3 and the LOCOS oxide film 2 is about -100nm as shown in drawing 13 The film 41 accumulates. WSix at this time The deposition conditions of the film 41 are Cold Wall. Using a mold CVD system, temperature is set into 680 degrees C, a pressure is set to 40Pa, and it considers as the flow rate of 100/1.6/100sccm using the reactant gas of SiH<sub>2</sub> Cl<sub>2</sub> / WF<sub>6</sub> / Ar, respectively. WSix The presentation ratio of the film 41 is W:Si=1:3.0.

[0066] It is WSix here. The film 41 is Si Rich from a stoichiometric composition ratio. It has become. This is WSix at a next process. As, and B or Phos introduced into the film 41 The class and its Dose of an impurity [ like ] It is because the work function of the gate electrode of completion is controlled according to an amount.

[0067] Next, it is WSix as shown in drawing 14 . On the film 41, it is LP. - Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm by the CVD method The film 43 accumulates. For example, using a vertical mold CVD system, temperature is set into 760 degrees C, they set a pressure to .53Pa, and the deposition conditions of Si<sub>3</sub>N<sub>4</sub> film 43 at this time are SiH<sub>2</sub> Cl<sub>2</sub> / NH<sub>3</sub> / N<sub>2</sub>. It considers as the flow rate of 90/600/500sccm using reactant gas, respectively. This Si<sub>3</sub>N<sub>4</sub> The film 43 is film for controlling the out-diffusion of B from the gate electrode upper part.

[0068] Next, as shown in drawing 15 , it is Si<sub>3</sub>N<sub>4</sub>. WSix which the photoresist film 45 is formed on the film 43, and serves as a gate electrode by using this photoresist film 45 as a mask The impurity of B+Ion47 grade is doped by the film 41 by the ion implantation. Under the present circumstances, in order to produce to coincidence the gate electrode (that is, transistor from which a threshold V<sub>th</sub> differs) with which work functions differ in the same Wafer, the ion implantation to the gate is ion kinds and those Dose(s) by the resist mask. An amount has good control of striking a ball in any direction with each transistor from which V<sub>th</sub> differs.

[0069] Then, as shown in drawing 16 , the photoresist film 45 is removed, and on Si<sub>3</sub>N<sub>4</sub> film 43, thickness is SiO<sub>2</sub> which is about -150nm. The film 49 accumulates. This SiO<sub>2</sub> The film 49 is film for making it the ion implantation when forming a high-concentration diffusion layer not go into a gate electrode.

[0070] Here, it is this SiO<sub>2</sub>. Depositing at low temperature is desirable, for example, the film 49 is SiH<sub>4</sub>+O<sub>2</sub>. At 350-450 degrees C, deposition temperature deposits by the system of reaction with ordinary pressure CVD etc. It has good control of striking a ball in any direction with a resist mask at the process shown in drawing 15 , and

this is WSix. It is for making it the impurity by which the ion implantation was carried out into the film 41 not mutually spread in a longitudinal direction.

[0071] Next, it is SiO<sub>2</sub> as shown in drawing 17. The photoresist film 51 is formed on the film 49, and this photoresist film 51 has the pattern of a gate electrode.

[0072] Then, it is SiO<sub>2</sub>, using this photoresist film 51 as a mask, as shown in drawing 18. The film 49 and Si<sub>3</sub>N<sub>4</sub> Etching processing of the film 43 is carried out. SiO<sub>2</sub> at this time The film 49 and Si<sub>3</sub>N<sub>4</sub> The processing conditions of the film 43 are for example, the magnetron mold Etcher. It uses, and temperature is set into 20 degrees C, a pressure is set to 2.7Pa, and they are 1000W and CHF<sub>3</sub> about RFPower. A flow rate is set to 45sccm(s). Next, the photoresist film 51 is removed.

[0073] Next, it is SiO<sub>2</sub> as shown in drawing 19. It is WSix, using the film 49 as a mask. Etching processing of the film 41 is carried out. Thereby, gate oxide 3 is minded on a silicon substrate 1, and it is WSix. The gate electrode 41 which consists of film is formed. Then, the LDD layer which is not illustrated is formed in a silicon substrate 1 by introducing an impurity into the LDD field in a silicon substrate 1 which is not illustrated. In addition, installation of this impurity is with the case of N-MOSTr, and the case of P-MOSTr, and has good control of striking ion in any direction suitably using a resist mask.

[0074] Then, SiO<sub>2</sub> whose thickness Si<sub>3</sub>N<sub>4</sub> film 53a whose thickness is about 10nm accumulates on the whole surface (WSix it deposits in contact with the side attachment wall of the film 41), it continues, and is about 150nm on Si<sub>3</sub>N<sub>4</sub> film 53a as shown in drawing 20 Film 53b accumulates. next, this Si<sub>3</sub>N<sub>4</sub> Film 53a and SiO<sub>2</sub> Etch Back [ b / film 53] using anisotropy processing carrying out -- the gate electrode 41 and SiO<sub>2</sub> the side attachment wall of the film 49 -- SiO<sub>2</sub> / Si<sub>3</sub>N<sub>4</sub> from -- becoming LDD Spacer 53 is formed. Si<sub>3</sub>N<sub>4</sub> at this time The film and SiO<sub>2</sub> Both the deposition conditions and processing conditions of film 53b use what was described above. Here, it is LDD. They are SiO<sub>2</sub> / Si<sub>3</sub>N<sub>4</sub> about Spacer 53. The reason made into two-layer membrane structure is WSix in a next heat treatment process. It is for controlling the out-diffusion of the impurity from the side-attachment-wall part of the gate electrode 41.

[0075] Next, as shown in drawing 21, after depositing the thin oxide film 55 for channeling prevention on a silicon substrate 1, the photoresist film 57 is formed on a silicon substrate 1. The pattern configuration of this photoresist film 57 carries out opening of the source drain field formation section. Then, the diffusion layer of the source drain field which is not illustrated is formed by carrying out the installation 25 of an impurity, for example, the ion implantation of BF<sub>2</sub><sup>+</sup>, to a silicon substrate 1 by using this photoresist film 57 as a mask. In addition, the case of N-MOSTr, and in the case of P-MOSTr, this ion implantation is suitably had good control of striking in any direction using a resist mask.

[0076] Next, after removing the photoresist film 57, heat treatment for activating the gate electrode 41, a LDD layer, the diffusion layer of a source drain field, and other impurity installation layers is performed. For example, in Ar ambient atmosphere, temperature is made into 1000 degrees C, they make the processing time 10 seconds, and RTA processing is used for the heat treatment conditions at this time.

[0077] Then, as shown in drawing 22, it is SiO<sub>2</sub> in the usual process. An interlayer insulation film 61 accumulates on the film 49, Sideall Spacer 53, and a silicon substrate 1. Next, contact hole 61a is prepared in this interlayer insulation film 61, a gap is filled by metal 63, wiring 65 is formed on this metal 63, and the inside of this contact hole 61a completes a component.

[0078] WSix which serves as a gate electrode at the process shown in drawing 14 according to the gestalt of implementation of the above 3rd It is Si<sub>3</sub>N<sub>4</sub> as a diffusion barrier layer on the film 41. When an ion implantation etc. makes an impurity the gate electrode (WSix film) 41 at the process which forms the film 43 and is shown in next drawing 15, it is Si<sub>3</sub>N<sub>4</sub>. It has introduced through the film (diffusion barrier layer) 43. As shown in drawing 31 (a), before forming the diffusion barrier layer of an impurity, in a field with a resist mask in a gate electrode (silicide) For this reason, an ion kind, Dose It stops producing a problem as shown in drawing 31 (b) called the spatial redistribution of the out-diffusion of the impurity in the gate electrode in the thermal process at the time of formation of the problem produced when an impurity is had good control of striking in any direction by V<sub>th</sub> which makes an amount the aim of Tr and it introduces, i.e., this diffusion barrier layer, or a longitudinal direction.

[0079] That is, after introducing an impurity into a gate electrode like the gestalt of the 2nd operation When depositing using the Si<sub>3</sub>N<sub>4</sub> CVD method which is the thin film which has the barrier nature to diffusion of an impurity It is LP on a gate electrode about the film. - (Si<sub>3</sub>N<sub>4</sub> by LP-CVD method the film is most excellent in respect of the diffusion barrier nature of an impurity, or the controllability of thickness.) Or WSix By nitriding a gate electrode directly, WN on the front face of a gate electrode in forming the becoming film Since all need an about 800-degree C elevated temperature for formation of a diffusion barrier layer (Si<sub>3</sub>N<sub>4</sub> the film and WN film),

the spatial redistribution of the out-diffusion of the impurity in a gate electrode or a longitudinal direction poses a problem. That is, it is the case of a process as shown in drawing 32 (a). However, with the gestalt of the 3rd operation, since the impurity is introduced into the gate electrode 41 after forming the diffusion barrier layer (Si<sub>3</sub>N<sub>4</sub> film) 43 of the impurity in a gate electrode, neither the out-diffusion of the impurity in a gate electrode nor the problem of lateral spatial redistribution is produced. That is, it is the case of a process as shown in drawing 32 (b).

[0080] Therefore, the ion kind which carries out an ion implantation to the gate electrode 41 and its Dose It becomes possible to obtain the refractory metal silicide gate electrode which has with an amount the work function correctly made into an aim. Especially, it is WSix. The ion kind and Dose which are different in a Wafer side since the effect of the counter diffusion of the longitudinal direction of the impurity in a gate electrode can be lost When producing the gate electrode which introduces an amount and has a different work function, it becomes possible to control a work function correctly, without being influenced of mutual.

[0081] Moreover, it is not based on the formation approach of a thin film (diffusion barrier layer) or formation conditions (especially heat treatment process) which control the out-diffusion of the impurity of a gate electrode, but it becomes possible to obtain the refractory metal silicide gate electrode which has the high impurity concentration made into the purpose controlled correctly.

[0082] In addition, WSix by which it was formed on the Bulk Si substrate and the work function was controlled by the gestalt of implementation of the above 3rd It is also possible to apply this invention to manufacture of the semiconductor device which has other gate electrodes, although this invention is applied to manufacture of the MOS mold semiconductor device which has the gate electrode 41, for example, it is MoSix. It is also possible to apply this invention to manufacture of the semiconductor device which has the gate electrode which consists of refractory metal silicide [ like ]. This MoSix It is low Dose of  $-1 \times 10^{13} \text{cm}^{-2}$  like. When forming a gate electrode using silicide to which that work function changes from an amount a lot, especially this invention is effective. That is, when ion, such as a class of impurity which changes with locations, and different high impurity concentration, is had good control of striking in any direction to the gate electrode in order to produce Tr from which V<sub>th</sub> differs before forming a diffusion prevention layer (Si<sub>3</sub>N<sub>4</sub> film), the spatial redistribution of the out-diffusion of the impurity in a gate electrode or a longitudinal direction poses a big problem. It is Si<sub>3</sub>N<sub>4</sub> by LP-CVD. Auto-Doping when forming the film It is because it shifts from what also makes V<sub>th</sub> of Tr of completion an aim as a result of changing from the value which the spatial redistribution of high impurity concentration etc. produces through a gaseous phase, and the work function of a gate electrode makes an aim by this. However, if an impurity is introduced into the gate electrode 41 after forming a diffusion prevention layer (Si<sub>3</sub>N<sub>4</sub> film 43) like the gestalt of the 3rd operation, it will not be influenced of the thermal process at the time of formation of a diffusion prevention layer.

[0083] Moreover, although this invention is applied to the semiconductor device formed on the Bulk Si substrate 1, it is also possible to apply this invention to the semiconductor device formed in a SOI substrate.

[0084] Moreover, Si<sub>3</sub>N<sub>4</sub> which is the film which touches the gate electrode 41 and controls the out-diffusion of the impurity in the gate electrode 41 It is LP about film 53a. - Although it is made to deposit with a CVD method, it is also possible to nitride gate electrode 41 self directly and to grow up a refractory metal nitride (WN<sub>x</sub> film).

[0085] Moreover, all parameters, such as thickness of each thin film used in the gestalt of implementation of the above 3rd, are the example, and its design change is possible for any parameter suitably by the semiconductor device made into the purpose.

[0086] Drawing 23 - drawing 30 are the sectional views showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and the gestalt of this operation deposits the thin film for out-diffusion prevention of an impurity, after processing the refractory metal silicide of a gate electrode, and it explains the case where an ion implantation is performed to a gate electrode through this thin film.

[0087] First, as shown in drawing 23, the LOCOS oxide film 2 and Well which is not illustrated are prepared in a silicon substrate 1, and isolation is performed using this LOCOS oxide film 2, Well, etc. Next, on the front face of the silicon substrate 1 of a component field, gate oxide 3 is formed by the oxidizing [ thermally ] method (growth)

[0088] Then, WSix whose thickness it is thin to a gate electrode on gate oxide 3 and the LOCOS oxide film 2 is about -100nm as shown in drawing 24 The film 41 accumulates. WSix at this time The deposition conditions of the film 41 are the same as that of what was shown with the gestalt of the 3rd operation. WSix The presentation ratio of the film 41 is W:Si=1:3.0.

[0089] It is WSix here. The film 41 is Si Rich from a stoichiometric composition ratio. It has become. This is WSix

at a next process. As, and B or Phos introduced into the film 41 The class and its Dose of an impurity [ like ] It is because the work function of the gate electrode of completion is controlled according to an amount.

[0090] Next, it is WSix as shown in drawing 25 . The photoresist film 67 is formed on the film 41, and this photoresist film 67 has the pattern of a gate electrode.

[0091] Then, it is WSix, using this photoresist film 67 as a mask, as shown in drawing 26 . Etching processing of the film 41 is carried out. Next, the photoresist film 67 is removed.

[0092] Next, it is WSix as shown in drawing 27 . On the gate electrode 41 and a silicon substrate 1, it is LP. - Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm by the CVD method The film 43 accumulates. Si<sub>3</sub>N<sub>4</sub> at this time The deposition conditions of the film 43 are the same as that of what was shown with the gestalt of the 3rd operation. This Si<sub>3</sub>N<sub>4</sub> The film 43 is film for controlling the out-diffusion of the impurity from the gate electrode 41.

[0093] Next, the LDD layer which is not illustrated is formed in a silicon substrate 1 by introducing an impurity into the LDD field in a silicon substrate 1 which is not illustrated. In addition, installation of this impurity is with the case of N-MOSTr, and the case of P-MOSTr, and has good control of striking ion in any direction suitably using a resist mask.

[0094] Then, as shown in drawing 28 , in the whole surface, it is SiO<sub>2</sub>. The film 69 accumulates. next, this SiO<sub>2</sub> Etch Back [ film / 69 ] using anisotropy processing carrying out -- the side attachment wall of the gate electrode 41 -- Si<sub>3</sub>N<sub>4</sub> 43 -- minding -- SiO<sub>2</sub> from -- becoming LDD Spacer69 is formed. SiO<sub>2</sub> at this time Both the deposition conditions and processing conditions of the film 69 are the same as that of what was shown with the gestalt of the 3rd operation.

[0095] Next, as shown in drawing 29 , after depositing the thin oxide film 55 for channeling prevention on a silicon substrate 1, the photoresist film 57 is formed on a silicon substrate 1. The pattern configuration of this photoresist film 57 carries out opening of the source drain field formation section. Then, the impurity to the diffusion layer of the gate electrode 41 and the source drain field of a silicon substrate 1 is introduced by using this photoresist film 57 as a mask (ion implantation). In addition, the case of N-MOSTr, and in the case of P-MOSTr, this ion implantation is suitably had good control of striking in any direction using a resist mask.

[0096] Next, after removing the photoresist film 57, heat treatment for activating the gate electrode 41, a LDD layer, the diffusion layer of a source drain field, and other impurity installation layers is performed. For example, in Ar ambient atmosphere, temperature is made into 1000 degrees C, they make the processing time 10 seconds, and RTA processing is used for the heat treatment conditions at this time.

[0097] Then, as shown in drawing 30 , it is Si<sub>3</sub>N<sub>4</sub> in the usual process. An interlayer insulation film 61 accumulates on the film 43, Side all Spacer 69, and a silicon substrate 1. Next, contact hole 61a is prepared in this interlayer insulation film 61, a gap is filled by metal 63, wiring 65 is formed on this metal 63, and the inside of this contact hole 61a completes a component.

[0098] It is WSix at the process which is shown in drawing 26 according to the gestalt of implementation of the above 4th. It is Si<sub>3</sub>N<sub>4</sub> as a diffusion barrier layer on the gate electrode 41 at the process shown in drawing 27 after carrying out patterning of the film 41 and forming a gate electrode. The film 43 was formed and the impurity is introduced into the gate electrode 41 by the ion implantation etc. at the process of subsequent drawing 29 . Thereby, the work function of a gate electrode is decided according to high impurity concentration with one simple substance Tr, and fluctuation of the work function by the counter diffusion of the longitudinal direction of the impurity in a gate electrode is not produced.

[0099] That is, in introducing an impurity into this gate electrode by the ion implantation after processing of a gate electrode (refractory metal silicide film) and forming the impurity diffusion prevention film in this gate electrode after that, problems, such as out-diffusion of the impurity in a gate electrode, arise with the heat at the time of formation of this impurity diffusion prevention film. That is, it is the case of a process as shown in drawing 32 (c). However, with the gestalt of the 4th operation, since the impurity diffusion prevention film is formed before performing the ion implantation of an impurity on the refractory metal silicide film, neither the out-diffusion of the impurity in a gate electrode nor the problem of lateral spatial redistribution is produced. That is, it is the case of a process as shown in drawing 32 (d). Therefore, also in the gestalt of implementation of the above 4th, the same effectiveness as the gestalt of the 3rd operation can be acquired.

[0100] Moreover, in order to introduce the impurity to the diffusion layer of the gate electrode 41 and a source drain field at the process shown in drawing 29 , the ion kind introduced into a diffusion layer and the ion kind introduced into a gate electrode will become the same. Consequently, although some degrees of freedom on a process design will be lost, since a process can be simplified very much compared with the gestalt of the 3rd operation, the manufacturing cost of a semiconductor device can be lowered.

[0101] In addition, WSix by which it was formed on the Bulk Si substrate and the work function was controlled by the gestalt of implementation of the above 4th It is also possible to apply this invention to manufacture of the semiconductor device which has other gate electrodes, although this invention is applied to manufacture of the MOS mold semiconductor device which has the gate electrode 41, for example, it is MoSix. It is also possible to apply this invention to manufacture of the semiconductor device which has the gate electrode which consists of refractory metal silicide [ like ].

[0102] Moreover, although this invention is applied to the semiconductor device formed on the Bulk Si substrate 1, it is also possible to apply this invention to the semiconductor device formed in a SOI substrate.

[0103] Moreover, Si<sub>3</sub>N<sub>4</sub> which is the film which touches the gate electrode 41 and controls the out-diffusion of the impurity in the gate electrode 41 It is LP about the film 43. - Although it is made to deposit with a CVD method, it is also possible to nitride gate electrode 41 self directly and to grow up a refractory metal nitride (WNx film).

[0104] Moreover, all parameters, such as thickness of each thin film used in the gestalt of implementation of the above 3rd, are the example, and its design change is possible for any parameter suitably by the semiconductor device made into the purpose.

[0105]

[Effect of the Invention] According to invention which relates to claims 1-13 as explained above, the insulator layer which contains nitrogen in the upper part and the side-attachment-wall section of a gate electrode which introduced the high-concentration impurity is formed. Therefore, even when a thermal process is in the production process after forming a gate electrode, fluctuation of the work function of the gate electrode of the completion produced according to the thermal process can be suppressed, and variation in a threshold electrical potential difference can be made small.

[0106] Moreover, according to invention concerning claim 14, after forming the thin film for out-diffusion prevention of an impurity on the refractory metal silicide film, the impurity is introduced into the refractory metal silicide film through this thin film. Moreover, according to invention concerning claim 15, after carrying out pattern NINGU of the refractory metal silicide film, the thin film for out-diffusion prevention of an impurity was formed in all or some of gate electrode surface, and the impurity is introduced into this gate electrode through this thin film after that. Therefore, in order to control the out-diffusion of the impurity in a gate electrode, also in the process which forms a diffusion barrier layer at an elevated temperature comparatively, it is correctly controllable to the value with an eye on the high impurity concentration of a gate electrode.

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TECHNICAL FIELD

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[Field of the Invention] This invention relates to a semiconductor device and its manufacture approach. It is related with the semiconductor device which can maintain the property stabilized also after the semiconductor device which has the gate electrode with which B (boron) was doped especially went through the subsequent thermal process, and its manufacture approach. Moreover, it is related with the manufacture approach of a semiconductor device of having the refractory metal gate electrode with which the work function was controlled by the class of impurity introduced, and its concentration.

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PRIOR ART

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[Description of the Prior Art] It is known by using SOI (Silicon on Insulator) structure that full separation between components becomes easy and that control of a latch rise peculiar to a soft error or CMOS<sub>Tr</sub> will be attained. Moreover, examination about what the high speed and high-reliability-ization of CMOS<sub>Tr</sub> LSI are attained for using the SOI structure where the thickness of Si barrier layer is about 500nm has been performed comparatively early.

[0003] Recently, it has turned out that make Si layer on the front face of SOI thin to about 100 morenm, and it controls in the condition that the high impurity concentration of a channel is also comparatively low, and the further excellent engine performance, such as control of a short channel effect and improvement in the current drive capacity of MOST<sub>Tr</sub>, will be obtained if it is made conditions (perfect depletion mold) which the whole Si barrier layer depletion-izes mostly.

[0004] However, n+Poly Si used abundantly from the former When using as gate electrode material to NMOST<sub>Tr</sub>, in order to carry out the threshold electrical potential difference  $V_{th}$  near [ 0.5 - 1.0V ]  $T_r$  usual enhancement type, it is  $-10^{17}$ -/cm<sup>2</sup> about the high impurity concentration of a channel. It must carry out above. Then, in order to produce enhancement type  $T_r$  with a perfect depletion mold, examination which uses p+Poly Si (B-DOPOS) as a gate ingredient is performed in recent years.

[0005] Bulk Si to which detailed-ization progresses on the other hand It also sets to a device and is Poly Si of the above-mentioned n mold. N channel, NMOST<sub>Tr</sub> is received for the purpose of also using the work function of a gate electrode and adjusting  $V_{th}$ , since a P channel cannot form MOST<sub>Tr</sub> of a surface channel mold strong against a short channel effect in coincidence. To n+Poly Si and PMOST<sub>Tr</sub>, it is p+Poly Si. Dual Gate used, respectively A process is examined and it is for the first time.

[0006] Drawing 33 (a) is the expanded sectional view showing the gate electrode in the semiconductor device which is the sectional view showing the conventional semiconductor device, and shows drawing 33 (b) to drawing 33 (a), and its near part (field of A), and is p+Poly Si. After forming a gate electrode, the trouble produced by giving a heat treatment process is shown.

[0007] As shown in drawing 33 (a), the LOCOS oxide film 103 for performing isolation is formed in the front face of a silicon substrate 101. next, p+Poly Si which doped B through gate oxide 102 on the silicon substrate 101 (Dope) from -- the becoming gate electrode 105 forms -- having -- a this gate electrode 105 and silicon substrate 101 top -- SiO<sub>2</sub> from -- the becoming interlayer insulation film 107 is formed.

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EFFECT OF THE INVENTION

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[Effect of the Invention] According to invention which relates to claims 1-13 as explained above, the insulator layer which contains nitrogen in the upper part and the side-attachment-wall section of a gate electrode which introduced the high-concentration impurity is formed. Therefore, even when a thermal process is in the production process after forming a gate electrode, fluctuation of the work function of the gate electrode of the completion produced according to the thermal process can be suppressed, and variation in a threshold electrical potential difference can be made small.

[0106] Moreover, according to invention concerning claim 14, after forming the thin film for out-diffusion prevention of an impurity on the refractory metal silicide film, the impurity is introduced into the refractory metal silicide film through this thin film. Moreover, according to invention concerning claim 15, after carrying out pattern NINGU of the refractory metal silicide film, the thin film for out-diffusion prevention of an impurity was formed in all or some of gate electrode surface, and the impurity is introduced into this gate electrode through this thin film after that. Therefore, in order to control the out-diffusion of the impurity in a gate electrode, also in the process which forms a diffusion barrier layer at an elevated temperature comparatively, it is correctly controllable to the value with an eye on the high impurity concentration of a gate electrode.

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 TECHNICAL PROBLEM
 

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[Problem(s) to be Solved by the Invention] By the way, p+Poly Si which doped this B (Dope) When it uses as a gate electrode 105, depending on the thermal process after doping B to the gate electrode 105 SiO<sub>2</sub> whose B in the gate electrode 105 is an interlayer insulation film 107 as shown in drawing 33 (b) etc. -- a deposit (deposit 111 of B) -- carrying out -- and B -- comparatively -- quick -- SiO<sub>2</sub> Inside is diffused (diffusion 113 to the interlayer insulation film of B). For this reason, Poly Si The concentration of inner B falls and it is Poly Si. In depletion-izing \*\*\*\*, it is p+Poly Si by this. A work function will be changed. in addition, same SiO<sub>2</sub> it is -- even if -- it is enlarged [ the diffusion coefficient of B ] by the inside of the interlayer insulation film 107 which is inferior to compactness from gate oxide 102.

[0009] That is, since the degree of the diffusion 113 to the interlayer insulation film of B changes according to the temperature of a next thermal process consequently, variation arises also in change of the work function of the gate electrode 105. Therefore, this p+Poly Si The variation in each property which makes the start V<sub>th</sub> variation of the transistor used for the gate electrode 105 will increase.

[0010] Moreover, variation in each above property and p+Poly Si It is becoming still more difficult to form the component of the property which lessened the field internal division cloth of the work function of the gate, and was stabilized in respect of the following. p+Poly Si of the completion by fluctuation of the thermal process after introducing an impurity into a gate electrode p+Poly Si by difference of the thermal process at the time of manufacture by the difference between fluctuation of the property of a gate electrode and the type of a semiconductor device It is because the effectual temperature distribution within a Wafer side also increase by diameter-ization of macrostomia of not only fluctuation of a work function but the adoption of RTA (Rapid Thermal Anneal) with temperature distribution large especially in recent years and Wafer etc.

[0011] Consequently, this p+Poly Si V<sub>th</sub> of Tr which used this for the gate electrode corresponding to fluctuation of a work function will be changed in a field, and is becoming a big trouble on semiconductor device production for future low-battery-izing and low-power-izing. that is, -- if p+Poly Si (B-DOPOS) is used as a gate ingredient -- Channel -- Non-Dope it is -- V<sub>th</sub> is set a little to -1V to slight height by the case, and it is becoming a problem in the future device with which supply voltage falls for low-power-izing.

[0012] Moreover, the above troubles are p+Poly Si by which B was doped. Not only when it is the gate electrode of a monolayer, but SiO<sub>2</sub> W-Polycide which is the problem generally observed when using the gate electrode with which B which is an impurity with an inner large diffusion coefficient was doped for example, by which B was doped WSix by which the gate and B were doped The case of the monolayer gate etc. is also a common problem. That is, it is Doping to refractory metal silicide about an impurity like B. Since the diffusion coefficient of B in SiO<sub>2</sub> which are silicide and the insulator layer which usually encloses a gate electrode is very large when it carries out, even if it introduces B of a certain constant rate, B concentration in the silicide of completion will be changed according to a subsequent thermal process. Consequently, WSix of completion It is Dose of B about the work function of the gate. It was impossible to have controlled only by the amount to the work function made into an aim.

[0013] Moreover, WSix Examination which uses refractory metal silicide [ like ] by the monolayer, and adjusts V<sub>th</sub> of SOITr of a perfect depletion mold to a suitable value is also beginning to be performed. As for refractory metal silicide like WSix, generally, there is much what has the work function near [ Mid-Gap ] Si. the case where refractory metal silicide is used for the gate electrode of SOITr of a perfect depletion mold -- V<sub>th</sub> -- Channel -- Non-Dope it is -- it becomes --0.5V and a suitable value by -0.5V and P-MOS by N-MOS at the time.

[0014] furthermore, WSix MoSix refractory metal silicide [ like ] -- a gate electrode -- using -- the presentation -- a stoichiometric composition ratio -- Si Rich \*\* -- introducing B, when it carries out -- Non-Dope comparing

and introducing As to the p+Si side -- Non-Dope It has become clear that it compares and some of the work function can be adjusted to the n+Si side.

[0015] Moreover, about the  $V_{th}$  control of  $T_r$  by the impurity of Channel, the problem of increase of  $V_{th}$  dispersion by statistical fluctuation is pointed out from detailed-izing of  $T_r$  size, and reduction of the amount of impurities contained in the Channel section of  $T_r$  per [ in accordance with it ] piece. Although this is not the demand which approached like [ in SOITr of a perfect depletion mold ], it is a technique which can creep in the future and is needed.

[0016] As mentioned above, controlling correctly to the value of  $V_{th}$  with an eye on the semiconductor device which has  $T_r$  of  $V_{th}$  which has good control of striking the class of impurity and its concentration in any direction according to various kinds of  $T_r(s)$  by the ion implantation, and is different from a situation which was described when manufacturing the semiconductor device which has the refractory metal silicide gate electrode by which the work function was controlled is called for. That is, the manufacture approach of a suitable semiconductor device of not fluctuating Profile of the impurity in the gate electrode after an ion implantation is searched for.

[0017] The purpose of invention which this invention is made in consideration of the above situations, and relates to claims 1-13 is to offer the semiconductor device which suppressed fluctuation of the work function of the gate electrode of the completion produced according to that thermal process, and made small variation in a threshold electrical potential difference, and its manufacture approach, even when a thermal process is in the production process after forming the gate electrode which introduced the high-concentration impurity.

[0018] Moreover, the purpose of invention concerning claims 14-18 is also in the process which forms a diffusion barrier layer at an elevated temperature comparatively to offer the manufacture approach of a semiconductor device correctly controllable to the value with an eye on the high impurity concentration of a gate electrode, in order to control the out-diffusion of the impurity in a gate electrode.

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**MEANS**

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[Means for Solving the Problem] the semiconductor device concerning this invention was formed on the gate electrode which was formed through gate dielectric film on the semi-conductor substrate and which introduced the high-concentration impurity, the insulator layer or the electric conduction film containing the nitrogen formed in the upper part and the side attachment wall section of this gate electrode, and this insulator layer or the electric conduction film in order to solve the above-mentioned technical problem -- at least -- SiO<sub>2</sub> it is characterize by to provide the include interlayer insulation film.

[0020] Moreover, the manufacture approach of the semiconductor device concerning this invention The process which forms gate dielectric film on a semi-conductor substrate, and the process which deposits the electric conduction film on this gate dielectric film, The process which introduces an impurity into this electric conduction film, the process which deposits the insulator layer containing nitrogen on this electric conduction film, and by processing this insulator layer and the electric conduction film the process which leaves an insulator layer on the gate electrode which consists of this electric conduction film, the process which forms the insulator layer which contains nitrogen in the side attachment wall of this insulator layer and this gate electrode, and this insulator layer top -- SiO<sub>2</sub> from -- it is characterized by providing the process which deposits the becoming interlayer insulation film.

[0021] By the above-mentioned semiconductor device and its manufacture approach, the insulator layer containing nitrogen is formed on the gate electrode which introduced the high-concentration impurity, and the insulator layer which contains nitrogen in the side attachment wall of a gate electrode is formed. For this reason, even if a thermal process is in the production process after forming a gate electrode, the impurity in a gate electrode is SiO<sub>2</sub> in that case. It can control being spread in the direction of the included interlayer insulation film. Therefore, the impurity introduced into the gate electrode can be activated effectively, fluctuation by the thermal process of the work function of the gate electrode of completion is suppressed, and variation in a threshold electrical potential difference can be made small.

[0022] Moreover, the manufacture approach of the semiconductor device concerning this invention is characterized by providing the process which forms gate dielectric film on a semi-conductor substrate, the process which deposits the refractory metal silicide film on this gate dielectric film, the process which forms the thin film for out-diffusion prevention of an impurity on this refractory metal silicide film, and the process which introduces an impurity into this refractory metal silicide film through this thin film.

[0023] By the manufacture approach of the above-mentioned semiconductor device, after forming the thin film for out-diffusion prevention of an impurity on the refractory metal silicide film, the impurity is introduced into the refractory metal silicide film through this thin film. The problem produced when an impurity is introduced into the refractory metal silicide film (gate electrode) by this before forming the thin film for out-diffusion prevention as a diffusion barrier layer of an impurity is lost. That is, it is because the spatial redistribution of the out-diffusion of the impurity in the refractory metal silicide film by the thermal process at the time of formation of this thin film or a longitudinal direction can be controlled.

[0024] Moreover, the manufacture approach of the semiconductor device concerning this invention The process which forms gate dielectric film on a semi-conductor substrate, and the process which deposits the refractory metal silicide film on this gate dielectric film, It is characterized by providing the process which carries out pattern NINGU of this refractory metal silicide film, and forms a gate electrode, the process which forms the thin film for out-diffusion prevention of an impurity in all or some of these gate electrode surfaces, and the process which introduces an impurity into this gate electrode through this thin film.

[0025] By the manufacture approach of the above-mentioned semiconductor device, after carrying out pattern

NINGU of the refractory metal silicide film, the thin film for out-diffusion prevention of an impurity is formed in all or some of gate electrode surfaces, and an impurity is introduced into this gate electrode through this thin film after that. Thereby, the work function of a gate electrode is decided according to high impurity concentration with one simple substance Tr, and fluctuation of the work function by the counter diffusion of the longitudinal direction of the impurity in a gate electrode is not produced.

[0026]

[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained with reference to a drawing. Drawing 1 (a) is the sectional view showing the semiconductor device by the gestalt of implementation of the 1st of this invention. p+Poly Si by which B (boron) for which this semiconductor device is used with a semiconductor integrated circuit was doped from — it has the becoming gate electrode.

[0027] It is Bulk as shown in drawing 1 (a). The LOCOS oxide film 2 is formed in the front face of a silicon substrate 1. Gate oxide 3 is formed on the front face of the silicon substrate 1 between this LOCOS oxide-film 2, and the gate electrode 5 is formed on this gate oxide 3. This gate electrode 5 is Poly Si whose thickness is 150nm. It is formed with the film and is this Poly Si. It is doped in it in the amount of dose (Dose) whose B is about  $[5 \times 10^{15} \text{cm}^{-2}]$  two, and the film is p+. It is a mold. In addition, this Poly Si B concentration in the film is  $-3.3 \times 10^{20} \text{cm}^{-3}$ .

[0028] Si<sub>3</sub>N<sub>4</sub> whose thickness is about 150nm on the gate electrode 5 The film 7 is formed and it is Spacer in the side attachment wall of the gate electrode 5. Si<sub>3</sub>N<sub>4</sub> whose width of face is about 150nm Side Wall Spacer 9 which consists of film is formed. in addition, Si<sub>3</sub>N<sub>4</sub> the film 7 and Side Wall Spacer 9 — LPCVD (Low Pressure Chemical Vapor Deposition) — it is formed of law.

[0029] Si<sub>3</sub>N<sub>4</sub> the film 7, Side Wall Spacer 9, and LOCOS oxide-film 2 top — SiO<sub>2</sub> from — the becoming interlayer insulation film 11 is formed.

[0030] According to the gestalt of implementation of the above 1st, it is Si<sub>3</sub>N<sub>4</sub> on the gate electrode 5. The film 7 is formed and it is Si<sub>3</sub>N<sub>4</sub> to the side attachment wall of the gate electrode 5. Side Wall Spacer 9 which consists of film is formed. For this reason, even if a thermal process is in the production process after forming the gate electrode 5, it can control that B in the gate electrode 5 is spread in the direction of an interlayer insulation film (SiO<sub>2</sub>) 11 in that case (out-diffusion). Therefore, B doped to the gate electrode 5 can be activated effectively, the fluctuation (heterogeneity of a work function) by the thermal process of the work function of the gate electrode 5 of completion is suppressed, and variation in a threshold electrical potential difference can be made small.

[0031] Moreover, p+Poly Si of the work function stabilized since it was hard to be influenced of the thermal process after gate electrode 5 formation It becomes possible to form a gate electrode. Therefore, although the thermal processes given to it will also differ if the classes of semiconductor device to manufacture differ, the thermal process is embraced even in such a case, and it is p+Poly Si of completion. It can lose changing the work function of a gate electrode. Furthermore, even when the effectual temperature distribution within a Wafer side increase by large adoption of temperature distribution of RTA, diameter-ization of macrostomia of Wafer, etc., it is p+Poly Si of completion. The component of the property which lessened the field internal division cloth of the work function of a gate electrode, and was stabilized can be formed.

[0032] In addition, Poly Si by which B was doped with the gestalt of implementation of the above 1st WSix by which B was doped although the gate electrode 5 of a monolayer was used Poly Si WSix which is possible also for using the gate electrode of Polycide of two-layer structure and by which B was doped It is also possible to use the gate electrode of a silicide monolayer [ like ].

[0033] Moreover, although B concentration in the gate electrode 5 is set to  $-3.3 \times 10^{20} \text{cm}^{-3}$ , it is also possible for it not to be limited to this but to choose B concentration according to each device.

[0034] Moreover, Si<sub>3</sub>N<sub>4</sub> formed of LP-CVD as film which controls diffusion of B from the gate electrode 5 It is also possible to use an insulator layer like [ although film 7 and 9 is used ] the SiON film formed of Plasma CVD as film which controls diffusion of B from the gate electrode 5, and it is also possible to use conductive film like TiN formed by CVD or the Sputter method.

[0035] Moreover, although B within a solid-solution limit is doped to the gate electrode 5, it is also possible to dope sufficient B which exceeds a solid-solution limit to the gate electrode 5. Thus, when doping B exceeding a solid-solution limit and heat-treating to a silicon substrate (Wafer) for activating B in a gate electrode, even if there are temperature distribution of extent which is in a Wafer side, it is absorbed, and properties, such as a work function of each gate electrode of completion, are not changed, namely, the property of each gate electrode can be stabilized.

[0036] Moreover, it is Si<sub>3</sub>N<sub>4</sub> to the upper part and the side-attachment-wall section of the gate electrode 5. Although film 7 and 9 is formed, it is also possible to form the electric conduction film which contains nitrogen in the upper part and the side-attachment-wall section of the gate electrode 5.

[0037] Drawing 1 (b) is the sectional view of the semiconductor device in which the modification of the semiconductor device by the gestalt of the 1st operation shown in drawing 1 (a) is shown, gives the same sign to the same part as drawing 1 (a), and explains only a different part.

[0038] Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm on the gate electrode 5 Si<sub>3</sub>N<sub>4</sub> whose thickness the film 7 is formed and is about -10nm at the side attachment wall of the gate electrode 5 The film 9 is formed. Si<sub>3</sub>N<sub>4</sub> On the film 7, it is SiO<sub>2</sub>. The film 13 is formed and it is Si<sub>3</sub>N<sub>4</sub>. In the side face of the film 9, it is SiO<sub>2</sub>. The film 15 is formed. moreover, Si<sub>3</sub>N<sub>4</sub> SiH<sub>2</sub> Cl<sub>2</sub> usual in film 7 and 9 NH<sub>3</sub> LPCVD by the thermal reaction of mixed gas -- it is formed of law. In addition, it is the insulator layer and Spacer of OffSet of the upper part of the gate electrode 5, and the side-attachment-wall section in this way. They are SiO<sub>2</sub> / Si<sub>3</sub>N<sub>4</sub> as an insulator layer. It is the insulator layer and Spacer of OffSet to use the two-layer film. It is for considering as the value of a request of width of face.

[0039] Also in the above-mentioned modification, the same effectiveness as the gestalt of the 1st operation can be acquired.

[0040] moreover -- above -- Si<sub>3</sub>N<sub>4</sub> of the upper part of the gate electrode 5, and the side-attachment-wall section although thickness of film 7 and 9 is thin-film-ized to about -10nm -- usual SiH<sub>2</sub> Cl<sub>2</sub> NH<sub>3</sub> LPCVD by the thermal reaction of mixed gas -- Si<sub>3</sub>N<sub>4</sub> formed by law the film -- even if it is several nm thickness, it fully has the barrier property to diffusion of impurities, such as B.

[0041] Moreover, Si<sub>3</sub>N<sub>4</sub> The increment in the dielectric constant of an interlayer film can be suppressed by forming the thickness of film 7 and 9 thinly with about -10nm. For this reason, while being able to operate a semiconductor device more at high speed, it is high LP-Si<sub>3</sub>N<sub>4</sub> of stress. The fall of the dependability of the device by the film can be suppressed to the minimum. However, when using film like SiON by which stress and a presentation were controlled using Plasma CVD etc., even if it forms the SiON film comparatively thickly, the increment in stress or a dielectric constant can be disregarded.

[0042] Drawing 2 - drawing 11 are the sectional views showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and also show the production process for producing the structure of the gate electrode shown in drawing 1 (a).

[0043] First, as shown in drawing 2, the LOCOS oxide film 2 and Well which is not illustrated are prepared in a silicon substrate 1, and isolation is performed using this LOCOS oxide film 2, Well, etc. Next, on the front face of the silicon substrate 1 of a component field, gate oxide 3 is formed by the oxidizing [ thermally ] method (growth).

[0044] Then, Poly Si whose thickness it is thin to a gate electrode on gate oxide 3 and the LOCOS oxide film 2 is about -150nm as shown in drawing 3 The film 5 accumulates.

[0045] Next, it is Poly Si as shown in drawing 4. The photoresist film 21 is formed on the film 5. The pattern configuration of this photoresist film 21 carries out opening of the P-MOS section. Then, it is Poly Si, using this photoresist film 21 as a mask. B is doped by the film 5 by the ion implantation 23 of BF<sub>2</sub><sup>+</sup>.

[0046] In addition, in order to consider as the device of the surface channel mold with which the fall of the threshold electrical potential difference V<sub>th</sub> by the short channel effect cannot produce both N-MOSTr and P-MOSTr easily, it is n<sup>+</sup> to N-MOS. It is p<sup>+</sup> to the gate and P-MOS. It is necessary to adopt the gate, respectively. Therefore, the ion implantation to the gate is had good control of striking in any direction with a resist mask.

[0047] Then, as shown in drawing 5, the above-mentioned photoresist film 21 is removed, and it is p<sup>+</sup>PolySi. On the film 5, Si<sub>3</sub>N<sub>4</sub> film 7 whose thickness is about -150nm accumulates by the LPCVD method. Si<sub>3</sub>N<sub>4</sub> at this time For example, using a vertical mold CVD system, temperature is set into 760 degrees C, they set a pressure to 53Pa, and the deposition conditions of the film 7 are SiH<sub>2</sub> Cl<sub>2</sub> / NH<sub>3</sub> / N<sub>2</sub>. It considers as the flow rate of 90/600/500sccm using reactant gas, respectively.

[0048] Next, as shown in drawing 6, it is Si<sub>3</sub>N<sub>4</sub>. The photoresist film 25 is formed on the film 7, and this photoresist film 25 has the pattern of a gate electrode.

[0049] Then, it is Si<sub>3</sub>N<sub>4</sub>, using this photoresist film 25 as a mask, as shown in drawing 7. Etching processing of the film 7 is carried out. Si<sub>3</sub>N<sub>4</sub> at this time The processing conditions of the film 7 are for example, the magnetron mold Etcher. It uses, and temperature is set into 20 degrees C, a pressure is set to 2.7Pa, and they are 1000W and CHF<sub>3</sub> about RFPower. A flow rate is set to 45sccm(s). Next, the photoresist film 25 is removed.

[0050] Next, as shown in drawing 8, it is Si<sub>3</sub>N<sub>4</sub>. It is p<sup>+</sup>Poly Si, using the film 7 as a mask. Etching processing of

the film 5 is carried out. Thereby, gate oxide 3 is formed on a silicon substrate 1, and it is p+Poly Si. The gate electrode 5 which consists of film is formed. Then, the LDD layer which is not illustrated is formed in a silicon substrate 1 by introducing an impurity into the LDD field in a silicon substrate 1 which is not illustrated (ion implantation). In addition, an ion implantation is with the case of N-MOSTr, and the case of P-MOSTr, that is, the case of an N channel, and in the case of a P channel, it is necessary to have good control of striking it in any direction suitably using a resist mask.

[0051] Then, as shown in drawing 9, in the whole surface, it is Si<sub>3</sub>N<sub>4</sub>. The film accumulates. Next, this Si<sub>3</sub>N<sub>4</sub> Etch Back [ film ] using anisotropy processing By carrying out, it is Si<sub>3</sub>N<sub>4</sub> in the side attachment wall of the gate electrode 5. LDD which consists of film Spacer 9 is formed. Si<sub>3</sub>N<sub>4</sub> at this time Both membranous deposition conditions and processing conditions use the above-mentioned thing.

[0052] Next, after depositing the thin oxide film for channeling prevention which is not illustrated, as shown in drawing 10, the photoresist film 27 is formed on a silicon substrate 1. The pattern configuration of this photoresist film 27 carries out opening of the source drain field formation section. Then, the diffusion layer of the source drain field which is not illustrated is formed by carrying out the installation 29 of an impurity, for example, the ion implantation of BF<sub>2</sub><sup>+</sup>, to a silicon substrate 1 by using this photoresist film 27 as a mask. In addition, this ion implantation is with the case of N-MOSTr, and the case of P-MOSTr, that is, the case of an N channel, and in the case of a P channel, it is necessary to have good control of striking it in any direction suitably using a resist mask.

[0053] Next, after removing the photoresist film 27, heat treatment (annealing) for activating the gate electrode 5, a LDD layer, the diffusion layer of a source drain field, and other impurity installation layers is performed. For example, in Ar ambient atmosphere, temperature is made into 1000 degrees C, they make the processing time 10 seconds, and RTA processing is used for the heat treatment conditions at this time.

[0054] Then, as shown in drawing 11, it is Si<sub>3</sub>N<sub>4</sub> in the usual process. The film 7, SideWall An interlayer insulation film 11 accumulates on Spacer 9 and a silicon substrate 1. Next, contact hole 11a is prepared in this interlayer insulation film 11, a gap is filled by metal 31, wiring 33 is formed on this metal 31, and the inside of this contact hole 11a completes a component.

[0055] According to the gestalt of implementation of the above 2nd, it is Si<sub>3</sub>N<sub>4</sub> on the gate electrode 5. The film 7 is formed and it is Si<sub>3</sub>N<sub>4</sub> to the side attachment wall of the gate electrode 5. Side Wall Spacer 9 which consists of film is formed. For this reason, it can control that B in the gate electrode 5 is spread in the direction of an interlayer insulation film (SiO<sub>2</sub>) 11 in the case of the thermal process after forming the gate electrode 5 (out-diffusion). Therefore, B doped to the gate electrode 5 can be activated effectively, fluctuation by the thermal process of the work function of the gate electrode 5 of completion is suppressed, and variation in a threshold electrical potential difference can be made small.

[0056] moreover, p+Poly Si of the work function stabilized since it was hard to be influenced of the thermal process after gate electrode 5 formation from -- it becomes possible to form the becoming gate electrode 5. Therefore, although the thermal processes given to it will also differ if the classes of semiconductor device to manufacture differ, the thermal process is embraced even in such a case, and it is p+PolySi of completion. It can lose changing the work function of a gate electrode. Furthermore, even when the effectual temperature distribution within a Wafer side increase by large adoption of temperature distribution of RTA, diameter-ization of macrostomia of Wafer, etc., it is p+Poly Si of completion. The component of the property which lessened the field internal division cloth of the work function of a gate electrode, and was stabilized can be formed.

[0057] That is, it is Si<sub>3</sub>N<sub>4</sub> about a gate electrode. By surrounding by the insulator layer which controls diffusion of an impurity [ like ], it can prevent B in the gate electrode 5 after heat treatment decreasing by out-diffusion. That is, it is not concerned with the existence of heat treatment after gate electrode 5 formation, the height of heat treatment temperature, and the merits and demerits of heat treatment time amount, but B concentration in the gate electrode 5 can be maintained while it has been [ at the time of B dope ] high. For this reason, even if this thermal process changes or the effectual temperature distribution within the Wafer side in a thermal process get worse, fluctuation of B concentration in the gate electrode of completion can be made small.

[0058] In addition, Poly Si by which B was doped with the gestalt of implementation of the above 2nd It is WSix although the manufacture approach of the semiconductor device using the gate electrode 5 of a monolayer is explained. The thing using the gate electrode of Polycide of two-layer structure with Poly Si may be used, and it is WSix. The thing using the gate electrode of a silicide monolayer [ like ] may be used.

[0059] Moreover, although the device about Tr formed on the Bulk Si substrate 1 is used, it is also possible to use the device of SOI structure.

[0060] Moreover, it is Si<sub>3</sub>N<sub>4</sub> as an insulator layer for diffusion prevention. The film 7 and LDD Although the manufacture approach of the semiconductor device using Spacer 9 is explained For example, thin LP-Si<sub>3</sub>N<sub>4</sub> The film and SiO<sub>2</sub> If it combines and deposits with SiO<sub>2</sub> / Si<sub>3</sub>N<sub>4</sub> = 140 / 10nm The rest is the OffSet insulator layer and Side Wall Spacer of the gate. It is also possible to produce the semiconductor device shown in drawing 1 (b) only by changing some membranous processing conditions.

[0061] namely, Poly Si shown in drawing 5 a film 5 top -- LPCVD -- Si<sub>3</sub>N<sub>4</sub> whose thickness is about -150nm by law After depositing the film 7 As shown in drawing 9 , it is Si<sub>3</sub>N<sub>4</sub> to the whole surface. The film is deposited and it is this Si<sub>3</sub>N<sub>4</sub>. Etch Back [ film ] using anisotropy processing By carrying out, it is Si<sub>3</sub>N<sub>4</sub> to the side attachment wall of the gate electrode 5. LDD which consists of film Although Spacer 9 is formed Poly Si a film 5 top -- LPCVD -- thin Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm by law The film is deposited. This Si<sub>3</sub>N<sub>4</sub> SiO<sub>2</sub> whose thickness is about -140nm on the film After depositing the film, the side attachment wall of the gate electrode 5 -- LPCVD -- thin Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm by law the film -- forming -- further -- this Si<sub>3</sub>N<sub>4</sub> SiO<sub>2</sub> whose thickness is about -140nm at a membranous side attachment wall By forming the film It is Si<sub>3</sub>N<sub>4</sub> to the side attachment wall of the gate electrode 5. The film and SiO<sub>2</sub> LDD which consists of film Spacer Forming is also possible. moreover, LPCVD usual as mentioned above -- Si<sub>3</sub>N<sub>4</sub> formed by law if it is the film - the out-diffusion of impurities, such as B from a gate electrode, can fully be controlled by thickness (several nm or -10nm).

[0062] Moreover, although gate oxide 3 is formed by the oxidizing [ thermally ] method on the front face of a silicon substrate 1, it is also possible to form the gate dielectric film which consists of a nitriding oxide film which comes to nitride an oxide film on the front face of a silicon substrate 1. That is, although what is necessary is just to control the out-diffusion in the upper part and the side-attachment-wall section of the gate electrode 5 since B concentration in the gate electrode 5 falls by carrying out out-diffusion of the B doped by the gate electrode 5 through the interlayer insulation film 11 with a mainly large diffusion coefficient Preferably, in order to control the diffusion rate of B also about gate oxide 3, it is good to adopt the nitriding oxide film which comes to nitride an oxide film 3, to control further the fall of B concentration in the gate electrode 5, and to fully control fluctuation of the work function of the gate electrode 5 of completion etc.

[0063] It is WSix by which drawing 12 - drawing 22 are the sectional views showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and the work function with which the gestalt of this operation was formed on the Bulk Si substrate in this invention was controlled. It applies to manufacture of the MOS mold semiconductor device which has a gate electrode.

[0064] First, as shown in drawing 12 , the LOCOS oxide film 2 and Well which is not illustrated are prepared in a silicon substrate 1, and isolation is performed using this LOCOS oxide film 2, Well, etc. Next, on the front face of the silicon substrate 1 of a component field, gate oxide 3 is formed by the oxidizing [ thermally ] method (growth).

[0065] Then, WSix whose thickness it is thin to a gate electrode on gate oxide 3 and the LOCOS oxide film 2 is about -100nm as shown in drawing 13 The film 41 accumulates. WSix at this time The deposition conditions of the film 41 are Cold Wall. Using a mold CVD system, temperature is set into 680 degrees C, a pressure is set to 40Pa, and it considers as the flow rate of 100/1.6/100sccm using the reactant gas of SiH<sub>2</sub> Cl<sub>2</sub> / WF<sub>6</sub> / Ar, respectively. WSix The presentation ratio of the film 41 is W:Si=1:3.0.

[0066] It is WSix here. The film 41 is Si Rich from a stoichiometric composition ratio. It has become. This is WSix at a next process. As, and B or Phos introduced into the film 41 The class and its Dose of an impurity [ like ] It is because the work function of the gate electrode of completion is controlled according to an amount.

[0067] Next, it is WSix as shown in drawing 14 . On the film 41, it is LP. - Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm by the CVD method The film 43 accumulates. For example, using a vertical mold CVD system, temperature is set into 760 degrees C, they set a pressure to 53Pa, and the deposition conditions of Si<sub>3</sub>N<sub>4</sub> film 43 at this time are SiH<sub>2</sub> Cl<sub>2</sub> / NH<sub>3</sub> / N<sub>2</sub>. It considers as the flow rate of 90/600/500sccm using reactant gas, respectively. This Si<sub>3</sub>N<sub>4</sub> The film 43 is film for controlling the out-diffusion of B from the gate electrode upper part.

[0068] Next, as shown in drawing 15 , it is Si<sub>3</sub>N<sub>4</sub>. WSix which the photoresist film 45 is formed on the film 43, and serves as a gate electrode by using this photoresist film 45 as a mask The impurity of B+Ion47 grade is doped by the film 41 by the ion implantation. Under the present circumstances, in order to produce to coincidence the gate electrode (that is, transistor from which a threshold V<sub>th</sub> differs) with which work functions differ in the same Wafer, the ion implantation to the gate is ion kinds and those Dose(s) by the resist mask. An amount has good control of striking a ball in any direction with each transistor from which V<sub>th</sub> differs.

[0069] Then, as shown in drawing 16 , the photoresist film 45 is removed, and on Si<sub>3</sub>N<sub>4</sub> film 43, thickness is SiO<sub>2</sub>

which is about -150nm. The film 49 accumulates. This SiO<sub>2</sub> The film 49 is film for making it the ion implantation when forming a high-concentration diffusion layer not go into a gate electrode.

[0070] Here, it is this SiO<sub>2</sub>. Depositing at low temperature is desirable, for example, the film 49 is SiH<sub>4</sub>+O<sub>2</sub>. At 350-450 degrees C, deposition temperature deposits by the system of reaction with ordinary pressure CVD etc. It has good control of striking a ball in any direction with a resist mask at the process shown in drawing 15, and this is WSix. It is for making it the impurity by which the ion implantation was carried out into the film 41 not mutually spread in a longitudinal direction.

[0071] Next, it is SiO<sub>2</sub> as shown in drawing 17. The photoresist film 51 is formed on the film 49, and this photoresist film 51 has the pattern of a gate electrode.

[0072] Then, it is SiO<sub>2</sub>, using this photoresist film 51 as a mask, as shown in drawing 18. The film 49 and Si<sub>3</sub> N<sub>4</sub> Etching processing of the film 43 is carried out. SiO<sub>2</sub> at this time The film 49 and Si<sub>3</sub> N<sub>4</sub> The processing conditions of the film 43 are for example, the magnetron mold Etcher. It uses, and temperature is set into 20 degrees C, a pressure is set to 2.7Pa, and they are 1000W and CHF<sub>3</sub> about RFPower. A flow rate is set to 45sccm(s). Next, the photoresist film 51 is removed.

[0073] Next, it is SiO<sub>2</sub> as shown in drawing 19. It is WSix, using the film 49 as a mask. Etching processing of the film 41 is carried out. Thereby, gate oxide 3 is minded on a silicon substrate 1, and it is WSix. The gate electrode 41 which consists of film is formed. Then, the LDD layer which is not illustrated is formed in a silicon substrate 1 by introducing an impurity into the LDD field in a silicon substrate 1 which is not illustrated. In addition, installation of this impurity is with the case of N-MOSTr, and the case of P-MOSTr, and has good control of striking ion in any direction suitably using a resist mask.

[0074] Then, SiO<sub>2</sub> whose thickness Si<sub>3</sub> N<sub>4</sub> film 53a whose thickness is about 10nm accumulates on the whole surface (WSix it deposits in contact with the side attachment wall of the film 41), it continues, and is about 150nm on Si<sub>3</sub> N<sub>4</sub> film 53a as shown in drawing 20 Film 53b accumulates. next, this Si<sub>3</sub> N<sub>4</sub> Film 53a and SiO<sub>2</sub> Etch Back [ b / film 53] using anisotropy processing carrying out -- the gate electrode 41 and SiO<sub>2</sub> the side attachment wall of the film 49 -- SiO<sub>2</sub> / Si<sub>3</sub> N<sub>4</sub> from -- becoming LDD Spacer 53 is formed. Si<sub>3</sub> N<sub>4</sub> at this time The film and SiO<sub>2</sub> Both the deposition conditions and processing conditions of film 53b use what was described above. Here, it is LDD. They are SiO<sub>2</sub> / Si<sub>3</sub> N<sub>4</sub> about Spacer 53. The reason made into two-layer membrane structure is WSix in a next heat treatment process. It is for controlling the out-diffusion of the impurity from the side-attachment-wall part of the gate electrode 41.

[0075] Next, as shown in drawing 21, after depositing the thin oxide film 55 for channeling prevention on a silicon substrate 1, the photoresist film 57 is formed on a silicon substrate 1. The pattern configuration of this photoresist film 57 carries out opening of the source drain field formation section. Then, the diffusion layer of the source drain field which is not illustrated is formed by carrying out the installation 25 of an impurity, for example, the ion implantation of BF<sub>2</sub><sup>+</sup>, to a silicon substrate 1 by using this photoresist film 57 as a mask. In addition, the case of N-MOSTr, and in the case of P-MOSTr, this ion implantation is suitably had good control of striking in any direction using a resist mask.

[0076] Next, after removing the photoresist film 57, heat treatment for activating the gate electrode 41, a LDD layer, the diffusion layer of a source drain field, and other impurity installation layers is performed. For example, in Ar ambient atmosphere, temperature is made into 1000 degrees C, they make the processing time 10 seconds, and RTA processing is used for the heat treatment conditions at this time.

[0077] Then, as shown in drawing 22, it is SiO<sub>2</sub> in the usual process. An interlayer insulation film 61 accumulates on the film 49, Sideall Spacer 53, and a silicon substrate 1. Next, contact hole 61a is prepared in this interlayer insulation film 61, a gap is filled by metal 63, wiring 65 is formed on this metal 63, and the inside of this contact hole 61a completes a component.

[0078] WSix which serves as a gate electrode at the process shown in drawing 14 according to the gestalt of implementation of the above 3rd It is Si<sub>3</sub> N<sub>4</sub> as a diffusion barrier layer on the film 41. When an ion implantation etc. makes an impurity the gate electrode (WSix film) 41 at the process which forms the film 43 and is shown in next drawing 15, it is Si<sub>3</sub> N<sub>4</sub>. It has introduced through the film (diffusion barrier layer) 43. As shown in drawing 31 (a), before forming the diffusion barrier layer of an impurity, in a field with a resist mask in a gate electrode (silicide) For this reason, an ion kind, Dose It stops producing a problem as shown in drawing 31 (b) called the spatial redistribution of the out-diffusion of the impurity in the gate electrode in the thermal process at the time of formation of the problem produced when an impurity is had good control of striking in any direction by V<sub>th</sub> which makes an amount the aim of Tr and it introduces, i.e., this diffusion barrier layer, or a longitudinal direction.

[0079] That is, after introducing an impurity into a gate electrode like the gestalt of the 2nd operation When

depositing using the Si<sub>3</sub>N<sub>4</sub> CVD method which is the thin film which has the barrier nature to diffusion of an impurity. It is LP on a gate electrode about the film. – (Si<sub>3</sub>N<sub>4</sub> by LP-CVD method the film is most excellent in respect of the diffusion barrier nature of an impurity, or the controllability of thickness.) Or WSix By nitriding a gate electrode directly, WN on the front face of a gate electrode in forming the becoming film. Since all need an about 800-degree C elevated temperature for formation of a diffusion barrier layer (Si<sub>3</sub>N<sub>4</sub> the film and WN film), the spatial redistribution of the out-diffusion of the impurity in a gate electrode or a longitudinal direction poses a problem. That is, it is the case of a process as shown in drawing 32 (a). However, with the gestalt of the 3rd operation, since the impurity is introduced into the gate electrode 41 after forming the diffusion barrier layer (Si<sub>3</sub>N<sub>4</sub> film) 43 of the impurity in a gate electrode, neither the out-diffusion of the impurity in a gate electrode nor the problem of lateral spatial redistribution is produced. That is, it is the case of a process as shown in drawing 32 (b).

[0080] Therefore, the ion kind which carries out an ion implantation to the gate electrode 41 and its Dose It becomes possible to obtain the refractory metal silicide gate electrode which has with an amount the work function correctly made into an aim. Especially, it is WSix. The ion kind and Dose which are different in a Wafer side since the effect of the counter diffusion of the longitudinal direction of the impurity in a gate electrode can be lost. When producing the gate electrode which introduces an amount and has a different work function, it becomes possible to control a work function correctly, without being influenced of mutual.

[0081] Moreover, it is not based on the formation approach of a thin film (diffusion barrier layer) or formation conditions (especially heat treatment process) which control the out-diffusion of the impurity of a gate electrode, but it becomes possible to obtain the refractory metal silicide gate electrode which has the high impurity concentration made into the purpose controlled correctly.

[0082] In addition, WSix by which it was formed on the Bulk Si substrate and the work function was controlled by the gestalt of implementation of the above 3rd. It is also possible to apply this invention to manufacture of the semiconductor device which has other gate electrodes, although this invention is applied to manufacture of the MOS mold semiconductor device which has the gate electrode 41, for example, it is MoSix. It is also possible to apply this invention to manufacture of the semiconductor device which has the gate electrode which consists of refractory metal silicide [ like ]. This MoSix It is low Dose of  $-1 \times 10^{13} \text{cm}^{-2}$  like. When forming a gate electrode using silicide to which that work function changes from an amount a lot, especially this invention is effective. That is, when ion, such as a class of impurity which changes with locations, and different high impurity concentration, is had good control of striking in any direction to the gate electrode in order to produce  $T_r$  from which  $V_{th}$  differs before forming a diffusion prevention layer (Si<sub>3</sub>N<sub>4</sub> film), the spatial redistribution of the out-diffusion of the impurity in a gate electrode or a longitudinal direction poses a big problem. It is Si<sub>3</sub>N<sub>4</sub> by LP-CVD. Auto-Doping when forming the film. It is because it shifts from what also makes  $V_{th}$  of  $T_r$  of completion an aim as a result of changing from the value which the spatial redistribution of high impurity concentration etc. produces through a gaseous phase, and the work function of a gate electrode makes an aim by this. However, if an impurity is introduced into the gate electrode 41 after forming a diffusion prevention layer (Si<sub>3</sub>N<sub>4</sub> film 43) like the gestalt of the 3rd operation, it will not be influenced of the thermal process at the time of formation of a diffusion prevention layer.

[0083] Moreover, although this invention is applied to the semiconductor device formed on the Bulk Si substrate 1, it is also possible to apply this invention to the semiconductor device formed in a SOI substrate.

[0084] Moreover, Si<sub>3</sub>N<sub>4</sub> which is the film which touches the gate electrode 41 and controls the out-diffusion of the impurity in the gate electrode 41. It is LP about film 53a. – Although it is made to deposit with a CVD method, it is also possible to nitride gate electrode 41 self directly and to grow up a refractory metal nitride (WNx film).

[0085] Moreover, all parameters, such as thickness of each thin film used in the gestalt of implementation of the above 3rd, are the example, and its design change is possible for any parameter suitably by the semiconductor device made into the purpose.

[0086] Drawing 23 – drawing 30 are the sectional views showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and the gestalt of this operation deposits the thin film for out-diffusion prevention of an impurity, after processing the refractory metal silicide of a gate electrode, and it explains the case where an ion implantation is performed to a gate electrode through this thin film.

[0087] First, as shown in drawing 23, the LOCOS oxide film 2 and Well which is not illustrated are prepared in a silicon substrate 1, and isolation is performed using this LOCOS oxide film 2, Well, etc. Next, on the front face of the silicon substrate 1 of a component field, gate oxide 3 is formed by the oxidizing [ thermally ] method (growth).

[0088] Then, WSix whose thickness it is thin to a gate electrode on gate oxide 3 and the LOCOS oxide film 2 is about -100nm as shown in drawing 24 The film 41 accumulates. WSix at this time The deposition conditions of the film 41 are the same as that of what was shown with the gestalt of the 3rd operation. WSix The presentation ratio of the film 41 is W:Si=1:3.0.

[0089] It is WSix here. The film 41 is Si Rich from a stoichiometric composition ratio. It has become. This is WSix at a next process. As, and B or Phos introduced into the film 41 The class and its Dose of an impurity [ like ] It is because the work function of the gate electrode of completion is controlled according to an amount.

[0090] Next, it is WSix as shown in drawing 25 . The photoresist film 67 is formed on the film 41, and this photoresist film 67 has the pattern of a gate electrode.

[0091] Then, it is WSix, using this photoresist film 67 as a mask, as shown in drawing 26 . Etching processing of the film 41 is carried out. Next, the photoresist film 67 is removed.

[0092] Next, it is WSix as shown in drawing 27 . On the gate electrode 41 and a silicon substrate 1, it is LP. - Si<sub>3</sub>N<sub>4</sub> whose thickness is about -10nm by the CVD method The film 43 accumulates. Si<sub>3</sub>N<sub>4</sub> at this time The deposition conditions of the film 43 are the same as that of what was shown with the gestalt of the 3rd operation. This Si<sub>3</sub>N<sub>4</sub> The film 43 is film for controlling the out-diffusion of the impurity from the gate electrode 41.

[0093] Next, the LDD layer which is not illustrated is formed in a silicon substrate 1 by introducing an impurity into the LDD field in a silicon substrate 1 which is not illustrated. In addition, installation of this impurity is with the case of N-MOSTr, and the case of P-MOSTr, and has good control of striking ion in any direction suitably using a resist mask.

[0094] Then, as shown in drawing 28 , in the whole surface, it is SiO<sub>2</sub>. The film 69 accumulates. next, this SiO<sub>2</sub> Etch Back [ film / 69 ] using anisotropy processing carrying out -- the side attachment wall of the gate electrode 41 -- Si<sub>3</sub>N<sub>4</sub> 43 -- minding -- SiO<sub>2</sub> from -- becoming LDD Spacer69 is formed. SiO<sub>2</sub> at this time Both the deposition conditions and processing conditions of the film 69 are the same as that of what was shown with the gestalt of the 3rd operation.

[0095] Next, as shown in drawing 29 , after depositing the thin oxide film 55 for channeling prevention on a silicon substrate 1, the photoresist film 57 is formed on a silicon substrate 1. The pattern configuration of this photoresist film 57 carries out opening of the source drain field formation section. Then, the impurity to the diffusion layer of the gate electrode 41 and the source drain field of a silicon substrate 1 is introduced by using this photoresist film 57 as a mask (ion implantation). In addition, the case of N-MOSTr, and in the case of P-MOSTr, this ion implantation is suitably had good control of striking in any direction using a resist mask.

[0096] Next, after removing the photoresist film 57, heat treatment for activating the gate electrode 41, a LDD layer, the diffusion layer of a source drain field, and other impurity installation layers is performed. For example, in Ar ambient atmosphere, temperature is made into 1000 degrees C, they make the processing time 10 seconds, and RTA processing is used for the heat treatment conditions at this time.

[0097] Then, as shown in drawing 30 , it is Si<sub>3</sub>N<sub>4</sub> in the usual process. An interlayer insulation film 61 accumulates on the film 43, Side all Spacer 69, and a silicon substrate 1. Next, contact hole 61a is prepared in this interlayer insulation film 61, a gap is filled by metal 63, wiring 65 is formed on this metal 63, and the inside of this contact hole 61a completes a component.

[0098] It is WSix at the process which is shown in drawing 26 according to the gestalt of implementation of the above 4th. It is Si<sub>3</sub>N<sub>4</sub> as a diffusion barrier layer on the gate electrode 41 at the process shown in drawing 27 after carrying out patterning of the film 41 and forming a gate electrode. The film 43 was formed and the impurity is introduced into the gate electrode 41 by the ion implantation etc. at the process of subsequent drawing 29 . Thereby, the work function of a gate electrode is decided according to high impurity concentration with one simple substance Tr, and fluctuation of the work function by the counter diffusion of the longitudinal direction of the impurity in a gate electrode is not produced.

[0099] That is, in introducing an impurity into this gate electrode by the ion implantation after processing of a gate electrode (refractory metal silicide film) and forming the impurity diffusion prevention film in this gate electrode after that, problems, such as out-diffusion of the impurity in a gate electrode, arise with the heat at the time of formation of this impurity diffusion prevention film. That is, it is the case of a process as shown in drawing 32 (c). However, with the gestalt of the 4th operation, since the impurity diffusion prevention film is formed before performing the ion implantation of an impurity on the refractory metal silicide film, neither the out-diffusion of the impurity in a gate electrode nor the problem of lateral spatial redistribution is produced. That is, it is the case of a process as shown in drawing 32 (d). Therefore, also in the gestalt of implementation of the above 4th, the same effectiveness as the gestalt of the 3rd operation can be acquired.

[0100] Moreover, in order to introduce the impurity to the diffusion layer of the gate electrode 41 and a source drain field at the process shown in drawing 29, the ion kind introduced into a diffusion layer and the ion kind introduced into a gate electrode will become the same. Consequently, although some degrees of freedom on a process design will be lost, since a process can be simplified very much compared with the gestalt of the 3rd operation, the manufacturing cost of a semiconductor device can be lowered.

[0101] In addition, WSix by which it was formed on the Bulk Si substrate and the work function was controlled by the gestalt of implementation of the above 4th It is also possible to apply this invention to manufacture of the semiconductor device which has other gate electrodes, although this invention is applied to manufacture of the MOS mold semiconductor device which has the gate electrode 41, for example, it is MoSix. It is also possible to apply this invention to manufacture of the semiconductor device which has the gate electrode which consists of refractory metal silicide [ like ].

[0102] Moreover, although this invention is applied to the semiconductor device formed on the Bulk Si substrate 1, it is also possible to apply this invention to the semiconductor device formed in a SOI substrate.

[0103] Moreover, Si<sub>3</sub>N<sub>4</sub> which is the film which touches the gate electrode 41 and controls the out-diffusion of the impurity in the gate electrode 41 It is LP about the film 43. - Although it is made to deposit with a CVD method, it is also possible to nitride gate electrode 41 self directly and to grow up a refractory metal nitride (WNx film).

[0104] Moreover, all parameters, such as thickness of each thin film used in the gestalt of implementation of the above 3rd, are the example, and its design change is possible for any parameter suitably by the semiconductor device made into the purpose.

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[Translation done.]

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DESCRIPTION OF DRAWINGS

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## [Brief Description of the Drawings]

[Drawing 1] Drawing 1 (a) is the sectional view showing the semiconductor device by the gestalt of implementation of the 1st of this invention, and drawing 1 (b) is the sectional view of the semiconductor device in which the modification of the semiconductor device by the gestalt of the 1st operation shown in drawing 1 R> 1 (a) is shown.

[Drawing 2] It is the sectional view showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention.

[Drawing 3] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 2 .

[Drawing 4] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 3 .

[Drawing 5] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 4 .

[Drawing 6] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 5 .

[Drawing 7] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 6 .

[Drawing 8] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 7 .

[Drawing 9] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 8 .

[Drawing 10] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 9 .

[Drawing 11] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of implementation of the 2nd of this invention, and showing the next process of drawing 10 .

[Drawing 12] It is the sectional view showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention.

[Drawing 13] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 12 .

[Drawing 14] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 13 .

[Drawing 15] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 14 .

[Drawing 16] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 15 .

[Drawing 17] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 16 .

[Drawing 18] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 17 .

[Drawing 19] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 18 .

[Drawing 20] It is the sectional view in which showing the manufacture approach of the semiconductor device by

the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 19 .

[Drawing 21] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 20 .

[Drawing 22] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 3rd of this invention, and showing the next process of drawing 21 .

[Drawing 23] It is the sectional view showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention.

[Drawing 24] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and showing the next process of drawing 23 .

[Drawing 25] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and showing the next process of drawing 24 .

[Drawing 26] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and showing the next process of drawing 25 .

[Drawing 27] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and showing the next process of drawing 26 .

[Drawing 28] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and showing the next process of drawing 27 .

[Drawing 29] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and showing the next process of drawing 28 .

[Drawing 30] It is the sectional view in which showing the manufacture approach of the semiconductor device by the gestalt of operation of the 4th of this invention, and showing the next process of drawing 29 .

[Drawing 31] Drawing 31 (a) is an ion kind and Dose in a field. It has good control of striking a ball in any direction by  $V_{th}$  which makes an amount the aim of  $T_r$ , and is  $WS_{ix}$ . It is the sectional view showing the condition after carrying out an ion implantation to the film. Drawing 31 (b)  $WS_{ix}$  shown in drawing 31 (a) Auto-Doping which is in the condition after forming the diffusion prevention layer of an impurity on the film, and let the gaseous phase pass  $WS_{ix}$  It is the sectional view showing the condition that the redistribution of an impurity has arisen, by longitudinal direction diffusion.

[Drawing 32] Drawing 32 (a) and (b) are drawings showing the manufacture approach of pouring in an impurity before processing of a gate electrode, and drawing 32 (c) and (d) are drawings showing the manufacture approach of pouring in an impurity after processing of a gate electrode.

[Drawing 33] Drawing 33 (a) is the sectional view showing the conventional semiconductor device, and drawing 33 (b) is the expanded sectional view showing the gate electrode in the semiconductor device shown in drawing 33 (a), and its near part (field of A).

[Description of Notations]

1 -- Bulk A silicon substrate (semi-conductor substrate), 2 -- LOCOS oxide film, 3 [ The film, 9 -- Side Wall Spacer ( $Si_3N_4$  film), ] -- Gate oxide, 5 -- A gate electrode, 7 --  $Si_3N_4$  11 [ Film, ] -- An interlayer insulation film, 11a -- 13 A contact hole, 15 --  $SiO_2$  21 -- The photoresist film, 23 -- 25 The ion implantation of  $BF_2^+$ , 27 -- Photoresist film, 29 [ --  $WS_{ix}$  / Film, ] -- The ion implantation of  $BF_2^+$ , 31 -- Metal, 33 -- Wiring, 41 43 --  $Si_3N_4$  The film, 45 -- The photoresist film, 47 -- B-Ion, 49 --  $SiO_2$  The film, 51 [ Spacer ( $SiO_2$  /  $Si_3N_4$  Side Wall Spacer), ] -- The photoresist film, 53 -- LDD 53 a-- $Si_3N_4$  The film and 53 b-- $SiO_2$  The film, 55 -- The thin oxide film for channeling prevention, 57 -- The photoresist film, 59 --  $BF_2^+$  ion, 61 -- Interlayer insulation film, 61a [ -- Photoresist film, ] -- A contact hole, 63 -- Metal, 65 -- Wiring, 67 69 --  $SiO_2$  The film, 101 [ -- A LOCOS oxide film, 105 / -- A gate electrode, 107 / -- An interlayer insulation film ( $SiO_2$ ) 111 / -- The deposit of B, 113 / -- Diffusion to the interlayer insulation film of B. ] -- A silicon substrate, 102 -- Gate oxide 1,103

[Translation done.]

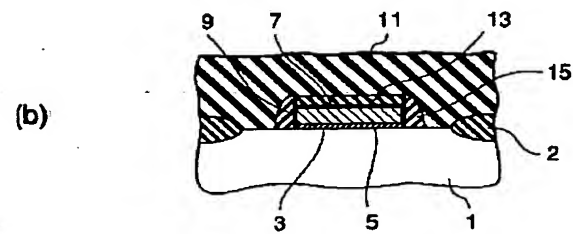
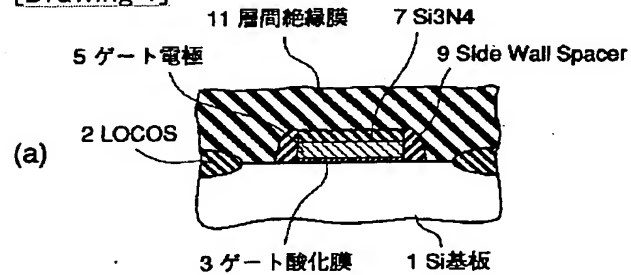
## \* NOTICES \*

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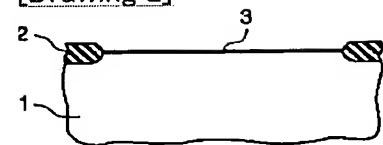
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- 2.\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

## DRAWINGS

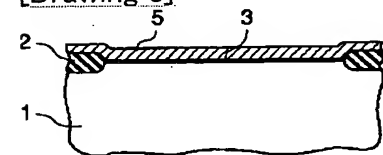
[Drawing 1]



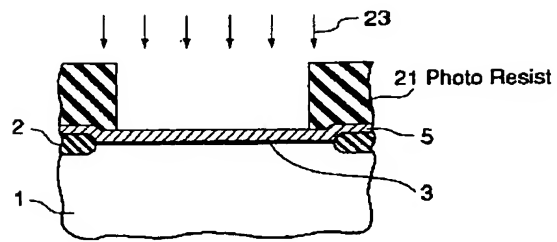
[Drawing 2]



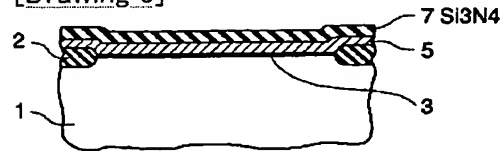
[Drawing 3]



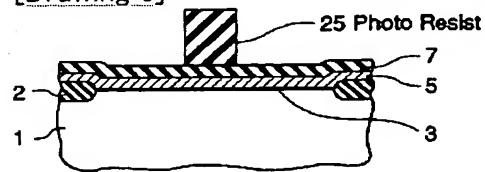
[Drawing 4]



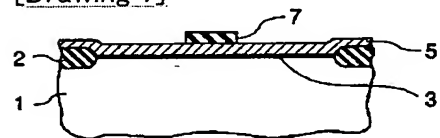
[Drawing 5]



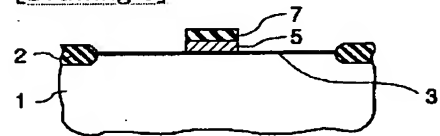
[Drawing 6]



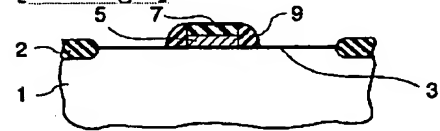
[Drawing 7]



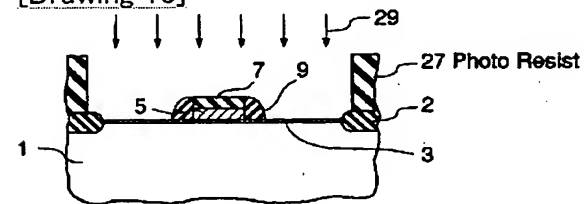
[Drawing 8]



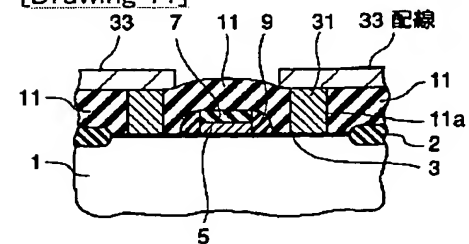
[Drawing 9]



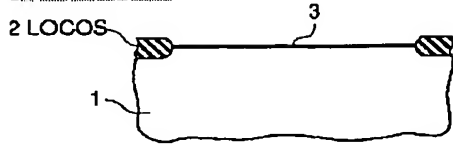
[Drawing 10]



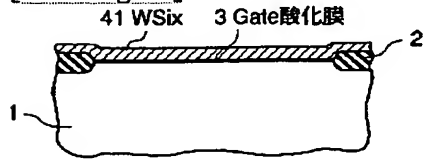
[Drawing 11]



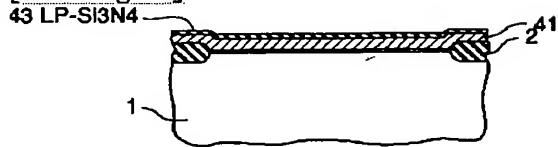
[Drawing 12]



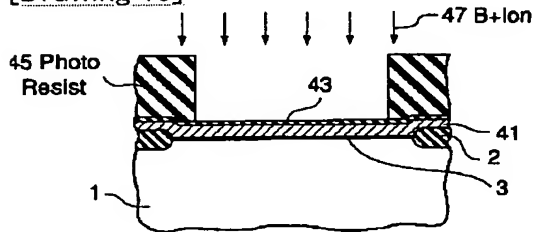
[Drawing 13]



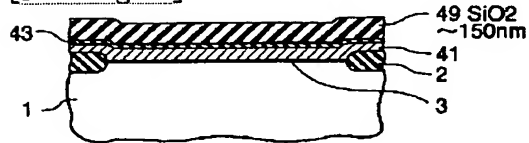
[Drawing 14]



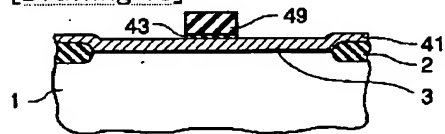
[Drawing 15]



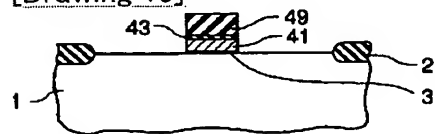
[Drawing 16]



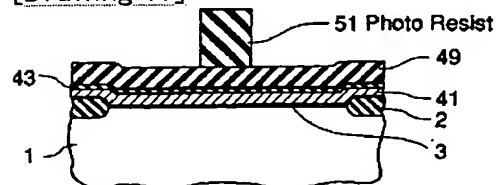
[Drawing 18]



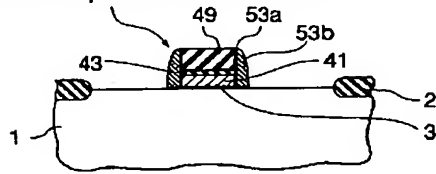
[Drawing 19]



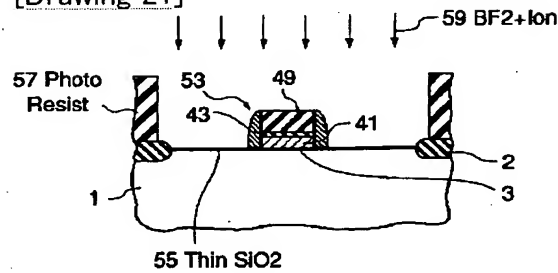
[Drawing 17]



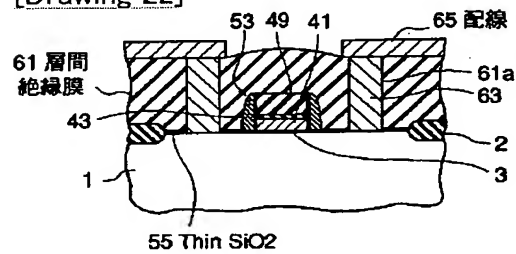
[Drawing 20]  
53 LDD Spacer SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> Stack



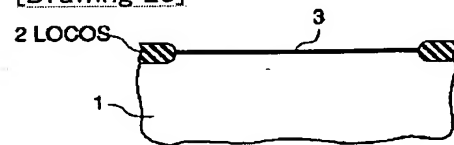
[Drawing 21]



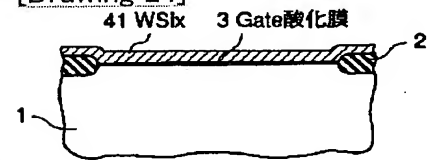
[Drawing 22]



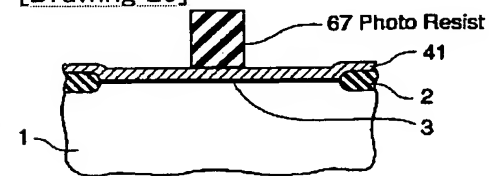
[Drawing 23]



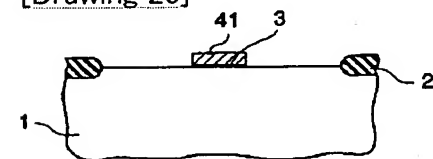
[Drawing 24]



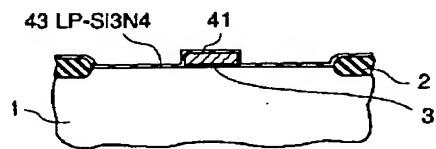
[Drawing 25]



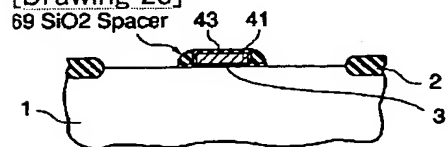
[Drawing 26]



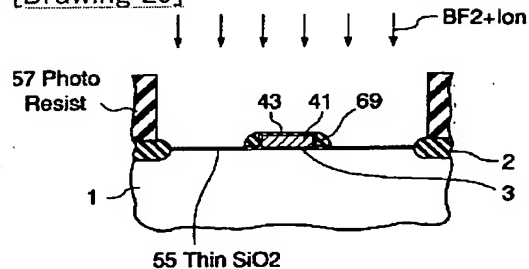
[Drawing 27]



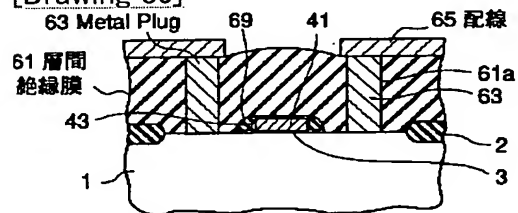
[Drawing 28]



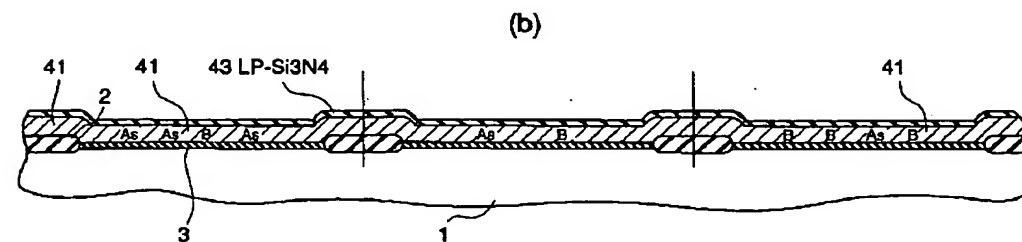
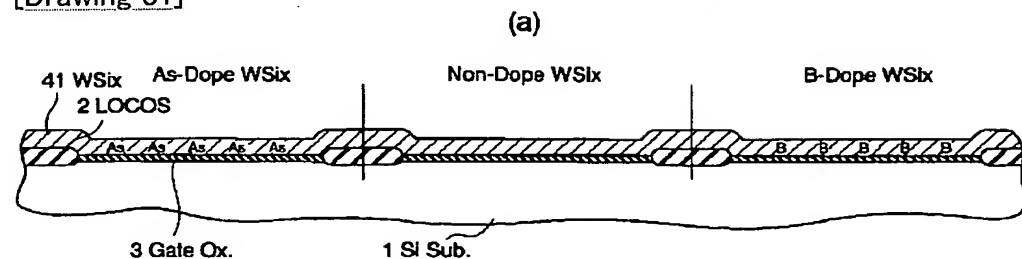
[Drawing 29]



[Drawing 30]



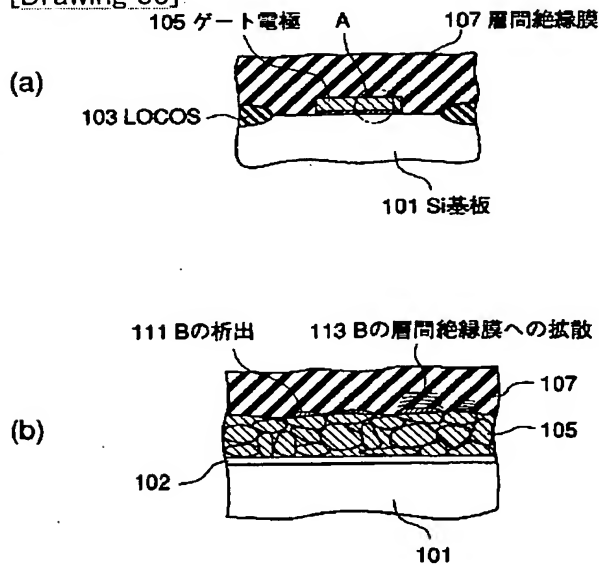
[Drawing 31]



[Drawing 32]



[Drawing 33]



[Translation done.]

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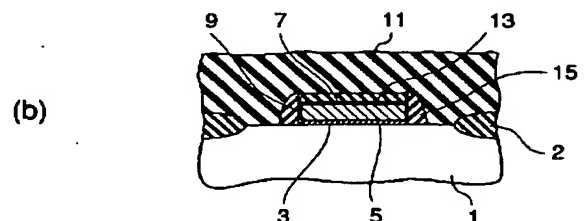
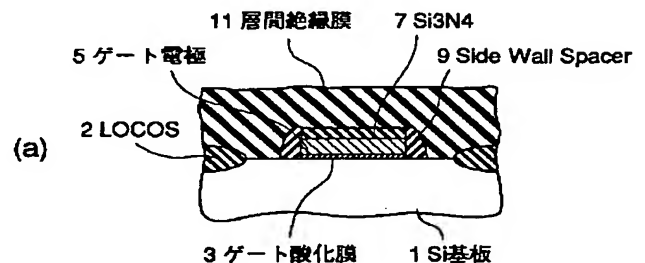
東京都品川区北品川6丁目7番35号ソニー株式会社内

(54) 【発明の名称】 半導体装置及びその製造方法

(57) 【要約】

・【課題】 ゲート電極形成後の製造工程に熱プロセスがある場合でも、その熱プロセスによって生じる出来上りのゲート電極の仕事関数の変動を抑えてしきい値電圧のバラツキを小さくした半導体装置及びその製造方法を提供する。

・【解決手段】 シリコン基板1の表面上にゲート酸化膜3を形成し、ゲート酸化膜3の上にゲート電極5を形成する。ゲート電極5は膜厚がPoly Si 膜によって形成されたもので、このPoly Si 膜の中にはBがドーパされp<sup>+</sup>型になっている。ゲート電極5の上にSi<sub>3</sub>N<sub>4</sub>膜7を形成し、ゲート電極5の側壁にSi<sub>3</sub>N<sub>4</sub>膜からなるSide Wall Spacer 9を形成する。Si<sub>3</sub>N<sub>4</sub>膜7、Side Wall Spacer 9およびLOCOS酸化膜2の上にSiO<sub>2</sub>からなる層間絶縁膜11を設ける。従って、ゲート電極5形成後の熱プロセスの際にゲート電極5中のBが層間絶縁膜11の方に拡散するのを抑制できる。



1

・【特許請求の範囲】

・【請求項 1】 半導体基板の上にゲート絶縁膜を介して形成された、高濃度の不純物を導入したゲート電極と、このゲート電極の上部及び側壁部に形成された窒素を含む絶縁膜又は導電膜と、この絶縁膜又は導電膜の上に形成された少なくとも  $\text{SiO}_2$  を含む層間絶縁膜と、を具備することを特徴とする半導体装置。

・【請求項 2】 上記ゲート電極が  $\text{p}^+\text{-Poly Si}$  からなることを特徴とする請求項 1 記載の半導体装置。

・【請求項 3】 上記ゲート電極が  $\text{WSi}_x$  と  $\text{Poly Si}$  との 2 層構造の Polycide からなることを特徴とする請求項 1 記載の半導体装置。

・【請求項 4】 上記ゲート電極がシリサイド単層からなることを特徴とする請求項 1 記載の半導体装置。

・【請求項 5】 上記不純物が B であることを特徴とする請求項 1 記載の半導体装置。

・【請求項 6】 上記窒素を含む絶縁膜が  $\text{LP-CVD}$  又は  $\text{Plasma CVD}$  により堆積された  $\text{Si}_3\text{N}_4$  膜又は  $\text{SiON}$  膜であることを特徴とする請求項 1 記載の半導体装置。

・【請求項 7】 上記窒素を含む絶縁膜が  $\text{LP-CVD}$  又は  $\text{Plasma CVD}$  により堆積された  $\text{Si}_3\text{N}_4$  膜又は  $\text{SiON}$  膜と  $\text{SiO}_2$  膜との 2 層構造の絶縁膜であることを特徴とする請求項 1 記載の半導体装置。

・【請求項 8】 上記ゲート絶縁膜が酸化膜を窒化してなる窒化酸化膜であることを特徴とする請求項 1 記載の半導体装置。

・【請求項 9】 半導体基板の上にゲート絶縁膜を形成する工程と、

このゲート絶縁膜の上に導電膜を堆積する工程と、この導電膜に不純物を導入する工程と、該導電膜の上に窒素を含む絶縁膜を堆積する工程と、この絶縁膜及び導電膜を加工することにより、該導電膜からなるゲート電極の上に絶縁膜を残す工程と、この絶縁膜及び該ゲート電極の側壁に窒素を含む絶縁膜を形成する工程と、

この絶縁膜の上に  $\text{SiO}_2$  からなる層間絶縁膜を堆積する工程と、

を具備することを特徴とする半導体装置の製造方法。

・【請求項 10】 上記不純物が B であることを特徴とする請求項 9 記載の半導体装置の製造方法。

・【請求項 11】 上記導電膜が  $\text{p}^+\text{-Poly Si}$  からなることを特徴とする請求項 9 記載の半導体装置の製造方法。

・【請求項 12】 上記窒素を含む絶縁膜が  $\text{LP-CVD}$  又は  $\text{Plasma CVD}$  により堆積された  $\text{Si}_3\text{N}_4$  膜又は  $\text{SiON}$  膜であることを特徴とする請求項 9 記載の半導体装置の製造方法。

・【請求項 13】 上記窒素を含む絶縁膜が  $\text{LP-CVD}$  又は  $\text{Plasma CVD}$  により堆積された  $\text{Si}_3\text{N}_4$  膜又は

2

$\text{SiON}$  膜と  $\text{SiO}_2$  膜との 2 層構造の絶縁膜であることを特徴とする請求項 9 記載の半導体装置の製造方法。

・【請求項 14】 半導体基板の上にゲート絶縁膜を形成する工程と、

このゲート絶縁膜の上に高融点金属シリサイド膜を堆積する工程と、

この高融点金属シリサイド膜上に不純物の外方拡散防止用の薄膜を形成する工程と、

この薄膜を通して該高融点金属シリサイド膜に不純物を導入する工程と、

を具備することを特徴とする半導体装置の製造方法。

・【請求項 15】 半導体基板の上にゲート絶縁膜を形成する工程と、

このゲート絶縁膜の上に高融点金属シリサイド膜を堆積する工程と、

この高融点金属シリサイド膜をパターンニングしてゲート電極を形成する工程と、

このゲート電極表面の全部又は一部に不純物の外方拡散防止用の薄膜を形成する工程と、

この薄膜を通して該ゲート電極に不純物を導入する工程と、

を具備することを特徴とする半導体装置の製造方法。

・【請求項 16】 上記外方拡散防止用の薄膜が、 $\text{LP-CVD}$  法によって形成される  $\text{Si}_3\text{N}_4$  膜であることを特徴とする請求項 14 又は 15 記載の半導体装置の製造方法。

・【請求項 17】 上記外方拡散防止用の薄膜が、該高融点金属シリサイド膜を直接窒化することによって形成される金属窒化物であることを特徴とする請求項 14 又は 15 記載の半導体装置の製造方法。

・【請求項 18】 上記高融点金属シリサイド膜が  $\text{WSi}_x$  膜もしくは  $\text{MoSi}_x$  膜であることを特徴とする請求項 14 又は 15 記載の半導体装置の製造方法。

・【発明の詳細な説明】

・【0001】

・【発明の属する技術分野】 本発明は、半導体装置及びその製造方法に関する。特に、B (ボロン) がドーピングされたゲート電極を有する半導体装置がその後の熱プロセスを経過した後でも安定した特性を維持することが可能な半導体装置及びその製造方法に関する。また、導入される不純物の種類およびその濃度により、仕事関数が制御された高融点金属ゲート電極を有する半導体装置の製造方法に関する。

・【0002】

・【従来の技術】  $\text{SOI}$  (Silicon on Insulator) 構造を用いることによって素子間同士の完全分離が容易になること、ソフトエラーや  $\text{CMOS Tr}$  に特有なラッチアップの抑制が可能になることが知られている。また、 $\text{Si}$  活性層の厚さが  $500\text{nm}$  程度の  $\text{SOI}$  構造を用いて  $\text{CMOS Tr LSI}$  の高速・高信頼性化を図ることについての

検討が比較的早くから行われてきた。

・【0003】最近では、SOI表面のSi層をさらに100nm程度にまで薄くし、チャネルの不純物濃度も比較的低い状態に制御して、ほぼSi活性層全体が空乏化するような条件（完全空乏型）にすると、短チャネル効果の抑制やMOSTrの電流駆動能力の向上などのさらに優れた性能が得られることがわかってきた。

・【0004】ところが、従来から多用されてきたn+Poly SiをNMOSTrに対するゲート電極材として用いる場合、そのしきい値電圧Vthを通常のエンハンスメント・タイプのTrの0.5～1.0V付近にするためには、チャネルの不純物濃度を $\sim 10^{17}/\text{cm}^2$ 以上にしなければならない。そこで、完全空乏型のままでエンハンスメント・タイプのTrを作製するために、ゲート材料としてp+Poly Si (B-DOP0S)を用いる検討が近年行われている。

・【0005】一方、微細化の進むBulk Siデバイスにおいても、上記のn型のPoly SiのみではNチャネル、Pチャネルとも同時に短チャネル効果に強い表面チャネル型のMOSTrを形成することができないためにゲート電極の仕事関数をも用いてVthを調整することを目的としてNMOSTrに対しては、n+Poly Si、PMOSTrに対しては、p+Poly Siをそれぞれ用いるDual Gateプロセスが検討され初めている。

・【0006】図33(a)は、従来の半導体装置を示す断面図であり、図33(b)は、図33(a)に示す半導体装置におけるゲート電極及びその近傍部分(Aの領域)を示す拡大断面図であって、p+Poly Siのゲート電極を形成した後に熱処理工程を施すことにより生じる問題点を示すものである。

・【0007】図33(a)に示すように、シリコン基板101の表面には素子分離を行うためのLOCOS酸化膜103が形成される。次に、シリコン基板101の上にはゲート酸化膜102を介してBをドーブ(Dope)したp+Poly Siからなるゲート電極105が形成され、このゲート電極105及びシリコン基板101の上にはSiO<sub>2</sub>からなる層間絶縁膜107が形成される。

・【0008】

・【発明が解決しようとする課題】ところで、このBをドーブ(Dope)したp+Poly Siをゲート電極105として用いた場合、ゲート電極105にBをドーブした後の熱プロセスによっては、図33(b)に示すように、ゲート電極105中のBが層間絶縁膜107であるSiO<sub>2</sub>等に析出(Bの析出111)し、かつBが比較的速くSiO<sub>2</sub>中を拡散(Bの層間絶縁膜への拡散113)していく。このため、Poly Si中のBの濃度が低下してPoly Siが空乏化したり、また、これによってp+Poly Siの仕事関数に変動したりしてしまう。尚、同じSiO<sub>2</sub>であってもゲート酸化膜102よりも緻密性に劣る層間絶縁膜107中はBの拡散係数が大きいとされている。

・【0009】つまり、Bの層間絶縁膜への拡散113の度合いが後の熱プロセスの温度に応じて変化するので、その結果、ゲート電極105の仕事関数の変化にもバラツキが生じる。したがって、このp+Poly Siをゲート電極105に用いたトランジスタのVthバラツキを初めとする各特性のバラツキが増大してしまう。

・【0010】また、上記のような各特性のバラツキ、p+Poly Siゲートの仕事関数の面内分布を少なくして安定した特性の素子を形成することは以下の点でますます難しくなっている。ゲート電極に不純物を導入した後の熱プロセスの変動による出来上りのp+Poly Siゲート電極の特性の変動、半導体装置のタイプの違いによる製造時の熱プロセスの相違によるp+Poly Siの仕事関数の変動のみならず、特に近年は温度分布の大きいRTA(Rapid Thermal Anneal)の採用やWaferの大口径化等によりWafer面内の実効的な温度分布も増大するようになっているからである。

・【0011】その結果、このp+Poly Siの仕事関数の変動に対応してこれをゲート電極に用いたTrのVthが面内で変動することになり、将来の低電圧化、低消費電力化のための半導体装置作製上の大きな問題点となりつつある。つまり、ゲート材料としてp+Poly Si (B-DOP0S)を用いると、ChannelがNon-Dopeの場合でVthが $\sim 1\text{V}$ とやや高めになってしまい、低消費電力化のために電源電圧が下がる将来のデバイスにおいて問題となってきた。

・【0012】また、上記のような問題点はBがドーブされたp+Poly Si単層のゲート電極の場合だけでなく、SiO<sub>2</sub>中の拡散係数の大きい不純物であるBがドーブされたゲート電極を用いる場合には一般的に観測される問題であり、例えばBがドーブされたW-PolycideゲートやBがドーブされたWSix単層ゲート等の場合も共通の問題である。つまり、Bのような不純物を高融点金属シリサイドにDopingした場合、シリサイドおよび通常ゲート電極を取り囲む絶縁膜であるSiO<sub>2</sub>中のBの拡散係数は非常に大きいため、ある一定量のBを導入してもその後の熱プロセスによっては出来上りのシリサイド中のB濃度が変動してしまう。その結果、出来上りのWSixゲートの仕事関数をBのDose量のみで狙いとする仕事関数に制御するのは不可能であった。

・【0013】また、例えばWSixのような高融点金属シリサイドを単層で用いて完全空乏型のSOITrのVthを適当な値に調整する検討も行われ始めている。WSixのような高融点金属シリサイドは一般にSiのMid-Gap近辺にその仕事関数を有するものが多い。完全空乏型のSOITrのゲート電極に高融点金属シリサイドを用いた場合、VthはChannelがNon-DopeのときのN-MOSで $\sim 0.5\text{V}$ 、P-MOSで $\sim -0.5\text{V}$ と適切な値になる。

・【0014】さらに、WSixやMoSixのような高

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融点金属シリサイドをゲート電極に用い、その組成を化学量論組成比よりもSi Richとした場合、Bを導入することによりNon-Dope に比べてp<sup>+</sup>・Si側へ、Asを導入することによりNon-Dope に比べてn<sup>+</sup>・Si側へ、その仕事関数を幾らか調整できることが判明している。

・【0015】また、Channelの不純物によるTrのVth制御については、Trサイズの微細化とそれに伴う1個当たりのTrのChannel部に含まれる不純物量の減少から統計的なゆらぎによるVthばらつきの増大の問題が指摘されている。これは、完全空乏型のSOITrの場合のように差し迫った要求ではないが、将来的にはいずれ必要となる技術である。

・【0016】以上、述べたような状況から、仕事関数が制御された高融点金属シリサイドゲート電極を有する半導体装置を製造する場合において、イオン注入により各種のTrに応じて不純物の種類およびその濃度を打ち分けて異なるVthのTrを有する半導体装置を狙いとするVthの値に正確に制御することが求められる。つまり、イオン注入後のゲート電極中の不純物のProfileを変動させない適切な半導体装置の製造方法が求められる。

・【0017】この発明は上記のような事情を考慮してなされたものであり、請求項1～13に係る発明の目的は、高濃度の不純物を導入したゲート電極を形成した後の製造工程に熱プロセスがある場合でも、その熱プロセスによって生じる出来上りのゲート電極の仕事関数の変動を抑えてしきい値電圧のバラツキを小さくした半導体装置及びその製造方法を提供することにある。

・【0018】また、請求項14～18に係る発明の目的は、ゲート電極中の不純物の外方拡散を抑制するために比較的高温にて拡散バリア層を形成するプロセスにおいても、ゲート電極の不純物濃度を狙いとする値に正確に制御できる半導体装置の製造方法を提供することにある。

・【0019】

・【課題を解決するための手段】この発明に係る半導体装置は、上記課題を解決するため、半導体基板の上にゲート絶縁膜を介して形成された、高濃度の不純物を導入したゲート電極と、このゲート電極の上部及び側壁部に形成された窒素を含む絶縁膜又は導電膜と、この絶縁膜又は導電膜の上に形成された少なくともSiO<sub>2</sub>を含む層間絶縁膜と、を具備することを特徴とする。

・【0020】また、この発明に係る半導体装置の製造方法は、半導体基板の上にゲート絶縁膜を形成する工程と、このゲート絶縁膜の上に導電膜を堆積する工程と、この導電膜に不純物を導入する工程と、該導電膜の上に窒素を含む絶縁膜を堆積する工程と、この絶縁膜及び導電膜を加工することにより、該導電膜からなるゲート電極の上に絶縁膜を残す工程と、この絶縁膜及び該ゲート電極の側壁に窒素を含む絶縁膜を形成する工程と、この絶縁膜の上にSiO<sub>2</sub>からなる層間絶縁膜を堆積する工

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程と、を具備することを特徴とする。

・【0021】上記半導体装置及びその製造方法では、高濃度の不純物を導入したゲート電極の上に窒素を含む絶縁膜を形成し、ゲート電極の側壁に窒素を含む絶縁膜を形成している。このため、ゲート電極を形成した後の製造工程に熱プロセスがあっても、その際にゲート電極中の不純物がSiO<sub>2</sub>を含む層間絶縁膜の方に拡散するのを抑制することができる。したがって、ゲート電極に導入した不純物を有効に活性化させることができ、出来上りのゲート電極の仕事関数の熱プロセスによる変動を抑えてしきい値電圧のバラツキを小さくできる。

・【0022】また、本発明に係る半導体装置の製造方法は、半導体基板の上にゲート絶縁膜を形成する工程と、このゲート絶縁膜の上に高融点金属シリサイド膜を堆積する工程と、この高融点金属シリサイド膜上に不純物の外方拡散防止用の薄膜を形成する工程と、この薄膜を通して該高融点金属シリサイド膜に不純物を導入する工程と、を具備することを特徴とする。

・【0023】上記半導体装置の製造方法では、高融点金属シリサイド膜上に不純物の外方拡散防止用の薄膜を形成した後に、この薄膜を通して高融点金属シリサイド膜に不純物を導入している。これにより、不純物の拡散バリア層としての外方拡散防止用の薄膜を形成する前に高融点金属シリサイド膜（ゲート電極）中に不純物を導入した場合に生じる問題はなくなる。つまり、この薄膜の形成時の熱プロセスによる高融点金属シリサイド膜中の不純物の外方拡散や横方向の空間的な再分布を抑制することができるからである。

・【0024】また、本発明に係る半導体装置の製造方法は、半導体基板の上にゲート絶縁膜を形成する工程と、このゲート絶縁膜の上に高融点金属シリサイド膜を堆積する工程と、この高融点金属シリサイド膜をパターンニングしてゲート電極を形成する工程と、このゲート電極表面の全部又は一部に不純物の外方拡散防止用の薄膜を形成する工程と、この薄膜を通して該ゲート電極に不純物を導入する工程と、を具備することを特徴とする。

・【0025】上記半導体装置の製造方法では、高融点金属シリサイド膜をパターンニングした後に、ゲート電極表面の全部又は一部に不純物の外方拡散防止用の薄膜を形成し、その後、この薄膜を通して該ゲート電極に不純物を導入する。これにより、1つの単体Trでゲート電極の仕事関数は不純物濃度に応じて決まり、ゲート電極中の不純物の横方向の相互拡散による仕事関数の変動は生じない。

・【0026】

・【発明の実施の形態】以下、図面を参照してこの発明の実施の形態を説明する。図1(a)は、この発明の第1の実施の形態による半導体装置を示す断面図である。この半導体装置は、半導体集積回路で用いられるB（ボロシ）がドーパされたp<sup>+</sup>・Poly Si からなるゲート電極を

有するものである。

・【0027】図1(a)に示すように、Bulk シリコン基板1の表面にはLOCOS酸化膜2が形成されている。このLOCOS酸化膜2相互間のシリコン基板1の表面上にはゲート酸化膜3が形成されており、このゲート酸化膜3の上にはゲート電極5が形成されている。このゲート電極5は膜厚が例えば150nmのPoly Si 膜によって形成されたものであり、このPoly Si 膜は其中にBが $5 \times 10^{15} \text{cm}^{-2}$ 程度のドーズ(Dose)量でドーブされp+型になっている。尚、このPoly Si 膜中のB濃度は $\sim 3.3 \times 10^{20} \text{cm}^{-3}$ である。

・【0028】ゲート電極5の上には厚さが $\sim 150 \text{nm}$ 程度の $\text{Si}_3\text{N}_4$ 膜7が形成されており、ゲート電極5の側壁にはSpacer 幅が例えば $\sim 150 \text{nm}$ 程度の $\text{Si}_3\text{N}_4$ 膜からなるSide Wall Spacer 9が形成されている。尚、 $\text{Si}_3\text{N}_4$ 膜7及びSide Wall Spacer 9はLPCVD(Low Pressure Chemical Vapor Deposition)法により形成されたものである。

・【0029】 $\text{Si}_3\text{N}_4$ 膜7、Side Wall Spacer 9およびLOCOS酸化膜2の上には $\text{SiO}_2$ からなる層間絶縁膜11が設けられている。

・【0030】上記第1の実施の形態によれば、ゲート電極5の上に $\text{Si}_3\text{N}_4$ 膜7を形成し、ゲート電極5の側壁に $\text{Si}_3\text{N}_4$ 膜からなるSide Wall Spacer 9を形成している。このため、ゲート電極5を形成した後の製造工程に熱プロセスがあっても、その際にゲート電極5中のBが層間絶縁膜( $\text{SiO}_2$ )11の方に拡散(外方拡散)するのを抑制することができる。したがって、ゲート電極5にドーブしたBを有効に活性化させることができ、出来上がりのゲート電極5の仕事関数の熱プロセスによる変動(仕事関数の不均一性)を抑えてしきい値電圧のバラツキを小さくできる。

・【0031】また、ゲート電極5形成後の熱プロセスの影響を受けにくいので、安定した仕事関数のp+ Poly Si のゲート電極を形成することが可能となる。したがって、製造する半導体装置の種類が異なれば、それに施される熱プロセスも異なることとなるが、その場合でもその熱プロセスに応じて出来上がりのp+ Poly Si のゲート電極の仕事関数が変動することを無くすることができる。さらに、温度分布の大きいRTAの採用やWaferの大口径化等によりWafer面内の実効的な温度分布が増大した場合でも、出来上がりのp+ Poly Si のゲート電極の仕事関数の面内分布を少なくして安定した特性の素子を形成できる。

・【0032】尚、上記第1の実施の形態では、BがドーブされたPoly Si 単層のゲート電極5を用いているが、BがドーブされたWSix とPoly Si との2層構造のPolycideのゲート電極を用いることも可能であり、BがドーブされたWSix のようなシリサイド単層のゲート電極を用いることも可能である。

・【0033】また、ゲート電極5中のB濃度を $\sim 3.3 \times 10^{20} \text{cm}^{-3}$ としているが、これに限定されず、それぞれのデバイスに応じてB濃度を選択することも可能である。

・【0034】また、ゲート電極5からのBの拡散を抑制する膜としてLP-CVDにより形成される $\text{Si}_3\text{N}_4$ 膜7、9を用いているが、ゲート電極5からのBの拡散を抑制する膜としてPlasma CVDにより形成される $\text{SiON}$ 膜のような絶縁膜を用いることも可能であり、CVD又はSputter法により形成されるTiNのような導電性の膜を用いることも可能である。

・【0035】また、ゲート電極5に固溶限以内のBをドーブしているが、ゲート電極5に固溶限を越える十分なBをドーブすることも可能である。このように固溶限を越えるBをドーブしておけば、ゲート電極中のBを活性化させるための熱処理をシリコン基板(Wafer)に施した際に、Wafer面内である程度の温度分布があったとしても、それを吸収して出来上がりのそれぞれのゲート電極の仕事関数等の特性が変動することがなく、即ちそれぞれのゲート電極の特性を安定化することができる。

・【0036】また、ゲート電極5の上部及び側壁部に $\text{Si}_3\text{N}_4$ 膜7、9を形成しているが、ゲート電極5の上部及び側壁部に窒素を含む導電膜を形成することも可能である。

・【0037】図1(b)は、図1(a)に示す第1の実施の形態による半導体装置の変形例を示す半導体装置の断面図であり、図1(a)と同一部分には同一符号を付し、異なる部分についてのみ説明する。

・【0038】ゲート電極5の上には膜厚が例えば $\sim 10 \text{nm}$ 程度の $\text{Si}_3\text{N}_4$ 膜7が形成されており、ゲート電極5の側壁には厚さが例えば $\sim 10 \text{nm}$ 程度の $\text{Si}_3\text{N}_4$ 膜9が形成されている。 $\text{Si}_3\text{N}_4$ 膜7の上には $\text{SiO}_2$ 膜13が形成されており、 $\text{Si}_3\text{N}_4$ 膜9の側面には $\text{SiO}_2$ 膜15が形成されている。また、 $\text{Si}_3\text{N}_4$ 膜7、9は通常の $\text{SiH}_2\text{Cl}_2$ と $\text{NH}_3$ との混合ガスの熱反応によるLPCVD法により形成されたものである。尚、このようにゲート電極5の上部及び側壁部のOffsetの絶縁膜やSpacerの絶縁膜として $\text{SiO}_2/\text{Si}_3\text{N}_4$ の2層膜を用いるのは、Offsetの絶縁膜やSpacer 幅を所望の値とするためである。

・【0039】上記変形例においても第1の実施の形態と同様の効果を得ることができる。

・【0040】また、上記のようにゲート電極5の上部及び側壁部の $\text{Si}_3\text{N}_4$ 膜7、9の膜厚を $\sim 10 \text{nm}$ 程度に薄膜化しているが、通常の $\text{SiH}_2\text{Cl}_2$ と $\text{NH}_3$ との混合ガスの熱反応によるLPCVD法により形成した $\text{Si}_3\text{N}_4$ 膜は $\sim$ 数nmの膜厚であってもB等の不純物の拡散に対するバリア性を十分に有している。

・【0041】また、 $\text{Si}_3\text{N}_4$ 膜7、9の膜厚を $\sim 10 \text{nm}$ 程度と薄く形成することにより、層間膜の誘電率の増

加を抑えることができる。このため、半導体装置をより高速で動作させることができるとともに、ストレスの高いLP-Si<sub>3</sub>N<sub>4</sub>膜によるデバイスの信頼性の低下を最小限に抑えることができる。但し、Plasma CVD等を用いてストレスや組成が制御されたSiONのような膜を用いる場合は、SiON膜を比較的厚く形成してもストレスや誘電率の増加は無視しうる。

・【0042】図2～図11は、この発明の第2の実施の形態による半導体装置の製造方法を示す断面図であり、図1(a)に示すゲート電極の構造を作製するための製造工程について示すものである。

・【0043】先ず、図2に示すように、シリコン基板1にはLOCOS酸化膜2及び図示せぬWellが設けられ、このLOCOS酸化膜2及びWell等を用いて素子分離が行われる。次に、素子領域のシリコン基板1の表面上には熱酸化法によりゲート酸化膜3が形成（成長）される。

・【0044】この後、図3に示すように、ゲート酸化膜3及びLOCOS酸化膜2の上にはゲート電極となる厚さが例えば～150nm程度のPoly Si膜5が堆積される。

・【0045】次に、図4に示すように、Poly Si膜5の上にはフォトレジスト膜21が形成される。このフォトレジスト膜21のパターン形状はP-MOS部を開口したものである。この後、このフォトレジスト膜21をマスクとしてPoly Si膜5にBが例えばBF<sub>2</sub><sup>+</sup>のイオン注入23によりドーピングされる。

・【0046】尚、N-MOSTrおよびP-MOSTrとともに短チャネル効果によるしきい値電圧V<sub>th</sub>の低下が生じにくい表面チャネル型のデバイスとするためには、N-MOSにn<sup>+</sup>ゲート、P-MOSにp<sup>+</sup>ゲートをそれぞれ採用する必要がある。従って、ゲートへのイオン注入はレジストマスクによって打ち分ける。

・【0047】この後、図5に示すように、上記フォトレジスト膜21が除去され、p<sup>+</sup>PolySi膜5の上にはLP-CVD法により例えば厚さが～150nm程度のSi<sub>3</sub>N<sub>4</sub>膜7が堆積される。この時のSi<sub>3</sub>N<sub>4</sub>膜7の堆積条件は、例えば縦型CVD装置を用い、温度を760℃、圧力を53Paとし、SiH<sub>2</sub>Cl<sub>2</sub>/NH<sub>3</sub>/N<sub>2</sub>の反応ガスを用い、それぞれ90/600/500sccmの流量とする。

・【0048】次に、図6に示すように、Si<sub>3</sub>N<sub>4</sub>膜7の上にはフォトレジスト膜25が設けられ、このフォトレジスト膜25はゲート電極のパターンを有するものである。

・【0049】この後、図7に示すように、このフォトレジスト膜25をマスクとしてSi<sub>3</sub>N<sub>4</sub>膜7がエッチング加工される。この時のSi<sub>3</sub>N<sub>4</sub>膜7の加工条件は、例えばマグネトロン型Etcherを用い、温度を20℃、圧力を2.7Paとし、RF Powerを1000W、CH

F<sub>3</sub>の流量を45sccmとする。次に、フォトレジスト膜25が除去される。

・【0050】次に、図8に示すように、Si<sub>3</sub>N<sub>4</sub>膜7をマスクとしてp<sup>+</sup>Poly Si膜5がエッチング加工される。これにより、シリコン基板1上にはゲート酸化膜3を介してp<sup>+</sup>Poly Si膜からなるゲート電極5が形成される。この後、シリコン基板1における図示せぬLDD領域に不純物を導入（イオン注入）することにより、シリコン基板1には図示せぬLDD層が形成される。尚、イオン注入は、N-MOSTrの場合とP-MOSTrの場合とで、つまりNチャネルの場合とPチャネルの場合とでレジストマスクを用いて適宜打ち分ける必要がある。

・【0051】この後、図9に示すように、全面にはSi<sub>3</sub>N<sub>4</sub>膜が堆積される。次に、このSi<sub>3</sub>N<sub>4</sub>膜を異方性加工を用いたEtch Backすることにより、ゲート電極5の側壁にはSi<sub>3</sub>N<sub>4</sub>膜からなるLDD Spacer 9が形成される。この時のSi<sub>3</sub>N<sub>4</sub>膜の堆積条件および加工条件は共に上記のものを用いる。

・【0052】次に、図示せぬチャネリング防止用の薄い酸化膜を堆積した後、図10に示すように、シリコン基板1の上にはフォトレジスト膜27が形成される。このフォトレジスト膜27のパターン形状はソース・ドレイン領域形成部を開口したものである。この後、このフォトレジスト膜27をマスクとしてシリコン基板1に不純物の導入、例えばBF<sub>2</sub><sup>+</sup>のイオン注入29をすることにより、図示せぬソース・ドレイン領域の拡散層が形成される。尚、このイオン注入は、N-MOSTrの場合とP-MOSTrの場合とで、つまりNチャネルの場合とPチャネルの場合とでレジストマスクを用いて適宜打ち分ける必要がある。

・【0053】次に、フォトレジスト膜27を除去した後、ゲート電極5、LDD層、ソース・ドレイン領域の拡散層、その他の不純物導入層を活性化させるための熱処理（アニール）が行われる。この時の熱処理条件は、例えばAr雰囲気中で温度を1000℃、処理時間を10秒とし、RTA処理を用いる。

・【0054】この後、図11に示すように、通常のプロセスにて、Si<sub>3</sub>N<sub>4</sub>膜7、SideWall Spacer 9、シリコン基板1の上には層間絶縁膜11が堆積される。次に、この層間絶縁膜11にはコンタクトホール11aが設けられ、このコンタクトホール11a内はメタル31により穴埋めされ、このメタル31の上には配線33が形成され、素子を完成させる。

・【0055】上記第2の実施の形態によれば、ゲート電極5の上にSi<sub>3</sub>N<sub>4</sub>膜7を形成し、ゲート電極5の側壁にSi<sub>3</sub>N<sub>4</sub>膜からなるSide Wall Spacer 9を形成している。このため、ゲート電極5を形成した後の熱プロセスの際にゲート電極5中のBが層間絶縁膜（SiO<sub>2</sub>）11の方に拡散（外方拡散）するのを抑制するこ

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とができる。したがって、ゲート電極5にドーブしたBを有効に活性化させることができ、出来上がりのゲート電極5の仕事関数の熱プロセスによる変動を抑えてしきい値電圧のバラツキを小さくできる。

・【0056】また、ゲート電極5形成後の熱プロセスの影響を受けにくいので、安定した仕事関数のp+ Poly Si からなるゲート電極5を形成することが可能となる。したがって、製造する半導体装置の種類が異なれば、それに施される熱プロセスも異なることとなるが、その場合でもその熱プロセスに応じて出来上がりのp+ Poly Si のゲート電極の仕事関数が変動することを無くすることができる。さらに、温度分布の大きいRTAの採用やWaferの大口径化等によりWafer面内の実効的な温度分布が増大した場合でも、出来上がりのp+ Poly Si のゲート電極の仕事関数の面内分布を少なくして安定した特性の素子を形成できる。

・【0057】すなわち、ゲート電極を例えばSi<sub>3</sub>N<sub>4</sub>のような不純物の拡散を抑制する絶縁膜で囲むことにより、熱処理後のゲート電極5中のBが外方拡散により減少するのを防ぐことができる。つまり、ゲート電極5形成後における熱処理の有無や熱処理温度の高低、熱処理時間の長短に関わらずゲート電極5中のB濃度をBドーブ時の高いままで維持することができる。このため、この熱プロセスが変化したり熱プロセスにおけるWafer面内の実効的な温度分布が悪化しても出来上がりのゲート電極中のB濃度の変動を小さくすることができる。

・【0058】尚、上記第2の実施の形態では、BがドーブされたPoly Si 単層のゲート電極5を用いた半導体装置の製造方法について説明しているが、WSix とPoly Siとの2層構造のPolycideのゲート電極を用いたものでも良いし、WSix のようなシリサイド単層のゲート電極を用いたものでも良い。

・【0059】また、Bulk Si 基板1上に形成されるT<sub>r</sub>についてのデバイスを用いているが、SOI構造のデバイスをを用いることも可能である。

・【0060】また、拡散防止のための絶縁膜としてSi<sub>3</sub>N<sub>4</sub>膜7及びLDD Spacer 9を用いた半導体装置の製造方法について説明しているが、例えば薄いLP-Si<sub>3</sub>N<sub>4</sub>膜とSiO<sub>2</sub>とを組合せてSiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>=140/10nmと堆積しておけば、後はゲートのOffset絶縁膜やSide Wall Spacer 膜の加工条件を多少変更するだけで図1(b)に示す半導体装置を作製することも可能である。

・【0061】すなわち、図5に示すPoly Si 膜5の上にLPCVD法により厚さが~150nm程度のSi<sub>3</sub>N<sub>4</sub>膜7を堆積した後、図9に示すように全面にSi<sub>3</sub>N<sub>4</sub>膜を堆積し、このSi<sub>3</sub>N<sub>4</sub>膜を異方性加工を用いたEtch Back することにより、ゲート電極5の側壁にSi<sub>3</sub>N<sub>4</sub>膜からなるLDD Spacer 9を形成しているが、Poly Si 膜5の上にLPCVD法により厚さが~1

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0nm程度の薄いSi<sub>3</sub>N<sub>4</sub>膜を堆積し、このSi<sub>3</sub>N<sub>4</sub>膜の上に厚さが~140nm程度のSiO<sub>2</sub>膜を堆積した後、ゲート電極5の側壁にLPCVD法により厚さが~10nm程度の薄いSi<sub>3</sub>N<sub>4</sub>膜を形成し、さらにこのSi<sub>3</sub>N<sub>4</sub>膜の側壁に厚さが~140nm程度のSiO<sub>2</sub>膜を形成することで、ゲート電極5の側壁にSi<sub>3</sub>N<sub>4</sub>膜及びSiO<sub>2</sub>膜からなるLDD Spacer を形成することも可能である。また、前述した通り通常のLPCVD法により形成したSi<sub>3</sub>N<sub>4</sub>膜であれば~数nm又は~10nmの膜厚でゲート電極からのB等の不純物の外方拡散を十分に抑制することができる。

・【0062】また、シリコン基板1の表面上に熱酸化法によりゲート酸化膜3を形成しているが、シリコン基板1の表面上に酸化膜を窒化してなる窒化酸化膜からなるゲート絶縁膜を形成することも可能である。つまり、ゲート電極5にドーブされたBは主に拡散係数の大きい層間絶縁膜11を通して外方拡散することによりゲート電極5中のB濃度が低下するので、ゲート電極5の上部及び側壁部での外方拡散を抑制すれば良いのであるが、好ましくは、ゲート酸化膜3についてもBの拡散速度を抑制するために酸化膜3を窒化してなる窒化酸化膜を採用して、ゲート電極5中のB濃度の低下をさらに抑制し、出来上がりのゲート電極5の仕事関数等の変動を十分に抑制するのが良い。

・【0063】図12~図22は、本発明の第3の実施の形態による半導体装置の製造方法を示す断面図であり、この実施の形態は、本発明をBulk Si 基板上に形成された仕事関数が制御されたWSix ゲート電極を有するMOS型半導体装置の製造に適用したものである。

・【0064】先ず、図12に示すように、シリコン基板1にはLOCOS酸化膜2及び図示せぬWell が設けられ、このLOCOS酸化膜2及びWell 等を用いて素子分離が行われる。次に、素子領域のシリコン基板1の表面上には熱酸化法によりゲート酸化膜3が形成(成長)される。

・【0065】この後、図13に示すように、ゲート酸化膜3及びLOCOS酸化膜2の上にはゲート電極となる厚さが例えば~100nm程度のWSix 膜41が堆積される。この時のWSix 膜41の堆積条件は、例えばCold Wall 型CVD装置を用い、温度を680℃、圧力を40Paとし、SiH<sub>2</sub>Cl<sub>2</sub>/WF<sub>6</sub>/Arの反応ガスを用い、それぞれ100/1.6/100sccmの流量とする。WSix 膜41の組成比はW:Si=1:3.0である。

・【0066】ここでWSix 膜41は、化学量論組成比よりもSi Rich となっている。これは、後の工程でWSix 膜41に導入されるAsやBもしくはPhos のような不純物の種類及びそのDose 量に応じて、出来上がりのゲート電極の仕事関数が制御される様にするためである。

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・【0067】次に、図14に示すように、WSix膜41の上にはLP-CVD法により厚さが例えば～10nm程度のSi<sub>3</sub>N<sub>4</sub>膜43が堆積される。この時のSi<sub>3</sub>N<sub>4</sub>膜43の堆積条件は、例えば縦型CVD装置を用い、温度を760℃、圧力を53Paとし、SiH<sub>2</sub>Cl<sub>2</sub>/NH<sub>3</sub>/N<sub>2</sub>の反応ガスを用い、それぞれ90/600/500sccmの流量とする。このSi<sub>3</sub>N<sub>4</sub>膜43はゲート電極上部からのBの外方拡散を抑制するための膜である。

・【0068】次に、図15に示すように、Si<sub>3</sub>N<sub>4</sub>膜43の上にはフォトレジスト膜45が形成され、このフォトレジスト膜45をマスクとしてゲート電極となるWSix膜41には例えばイオン注入によりB<sup>+</sup>Ion47等の不純物がドーブされる。この際、同一のWafer内に仕事関数の異なるゲート電極（つまり、しきい値V<sub>th</sub>の異なるトランジスタ）を同時に作製するため、ゲートへのイオン注入は、レジストマスクによってイオン種およびそれらのDose量がV<sub>th</sub>の異なるそれぞれのトランジスタで打ち分ける。

・【0069】この後、図16に示すように、フォトレジスト膜45は除去され、Si<sub>3</sub>N<sub>4</sub>膜43の上には厚さが例えば～150nm程度のSiO<sub>2</sub>膜49が堆積される。このSiO<sub>2</sub>膜49は、高濃度の拡散層を形成する時のイオン注入がゲート電極に入らないようにするための膜である。

・【0070】ここで、このSiO<sub>2</sub>膜49は、低温にて堆積するのが望ましく、例えば、SiH<sub>4</sub>+O<sub>2</sub>の反応系で堆積温度が350～450℃にて、常圧CVD等により堆積される。これは、図15に示す工程でレジストマスクで打ち分けられてWSix膜41中にイオン注入された不純物が横方向に相互に拡散しないようにするためである。

・【0071】次に、図17に示すように、SiO<sub>2</sub>膜49の上にはフォトレジスト膜51が形成され、このフォトレジスト膜51はゲート電極のパターンを有するものである。

・【0072】この後、図18に示すように、このフォトレジスト膜51をマスクとしてSiO<sub>2</sub>膜49及びSi<sub>3</sub>N<sub>4</sub>膜43がエッチング加工される。この時のSiO<sub>2</sub>膜49及びSi<sub>3</sub>N<sub>4</sub>膜43の加工条件は、例えばマグネトロン型Etcherを用い、温度を20℃、圧力を2.7Paとし、RF Powerを1000W、CHF<sub>3</sub>の流量を45sccmとする。次に、フォトレジスト膜51が除去される。

・【0073】次に、図19に示すように、SiO<sub>2</sub>膜49をマスクとしてWSix膜41がエッチング加工される。これにより、シリコン基板1上にはゲート酸化膜3を介してWSix膜からなるゲート電極41が形成される。この後、シリコン基板1における図示せぬLDD領域に不純物を導入することにより、シリコン基板1には

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図示せぬLDD層が形成される。尚、この不純物の導入は、N-MOSTrの場合とP-MOSTrの場合とで、レジストマスクを用いて適宜イオンを打ち分ける。

・【0074】この後、図20に示すように、全面には厚さが例えば10nm程度のSi<sub>3</sub>N<sub>4</sub>膜53aが堆積（WSix膜41の側壁に接して堆積）され、続いてSi<sub>3</sub>N<sub>4</sub>膜53aの上には厚さが例えば150nm程度のSiO<sub>2</sub>膜53bが堆積される。次に、このSi<sub>3</sub>N<sub>4</sub>膜53a及びSiO<sub>2</sub>膜53bを異方性加工を用いたEtch Backすることにより、ゲート電極41及びSiO<sub>2</sub>膜49の側壁にはSiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>からなるLDD Spacer 53が形成される。この時のSi<sub>3</sub>N<sub>4</sub>膜及びSiO<sub>2</sub>膜53bの堆積条件および加工条件は共に上記で述べたものを用いる。ここで、LDD Spacer 53をSiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>なる2層膜構造とする理由は、後の熱処理工程でのWSixゲート電極41の側壁部分からの不純物の外方拡散を抑制するためである。

・【0075】次に、図21に示すように、チャネリング防止用の薄い酸化膜55をシリコン基板1上に堆積した後、シリコン基板1の上にはフォトレジスト膜57が形成される。このフォトレジスト膜57のパターン形状はソース・ドレイン領域形成部を開口したものである。この後、このフォトレジスト膜57をマスクとしてシリコン基板1に不純物の導入、例えばBF<sub>2</sub><sup>+</sup>のイオン注入25をすることにより、図示せぬソース・ドレイン領域の拡散層が形成される。尚、このイオン注入は、N-MOSTrの場合とP-MOSTrの場合とでレジストマスクを用いて適宜打ち分ける。

・【0076】次に、フォトレジスト膜57を除去した後、ゲート電極41、LDD層、ソース・ドレイン領域の拡散層、その他の不純物導入層を活性化させるための熱処理が行われる。この時の熱処理条件は、例えばAr雰囲気中で温度を1000℃、処理時間を10秒とし、RTA処理を用いる。

・【0077】この後、図22に示すように、通常のプロセスにて、SiO<sub>2</sub>膜49、Sideall Spacer 53、シリコン基板1の上には層間絶縁膜61が堆積される。次に、この層間絶縁膜61にはコンタクトホール61aが設けられ、このコンタクトホール61a内はメタル63により穴埋めされ、このメタル63の上には配線65が形成され、素子を完成させる。

・【0078】上記第3の実施の形態によれば、図14に示す工程でゲート電極となるWSix膜41の上に拡散バリアー層としてのSi<sub>3</sub>N<sub>4</sub>膜43を形成し、この後の図15に示す工程でゲート電極（WSix膜）41に不純物をイオン注入等することによりSi<sub>3</sub>N<sub>4</sub>膜（拡散バリアー層）43を通して導入している。このため、図31(a)に示すように不純物の拡散バリアー層を形成する前にゲート電極（シリサイド）中にレジストマスクによって面内でイオン種、Dose量をTrの狙いとする

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る $V_{th}$ により不純物を打ち分けて導入した場合に生じる問題、即ちこの拡散バリアー層の形成時の熱プロセスにおけるゲート電極中の不純物の外方拡散や横方向の空間的な再分布という図31(b)に示すような問題は生じなくなる。

・【0079】つまり、第2の実施の形態のようなゲート電極に不純物を導入した後に、不純物の拡散に対するバリアー性を有する薄膜である $Si_3N_4$ 膜をゲート電極上にLP-CVD法を用いて堆積する場合(LP-CVD法による $Si_3N_4$ 膜は、不純物の拡散バリアー性や膜厚の制御性の点で最も優れている。)、又は、WSixゲート電極を直接窒化することによりゲート電極の表面にWNなる膜を形成する場合には、いずれも拡散バリアー層( $Si_3N_4$ 膜、WNなる膜)の形成に800℃程度の高温を必要とするため、ゲート電極中の不純物の外方拡散や横方向の空間的な再分布が問題となる。即ち図32(a)に示すような工程の場合である。しかし、第3の実施の形態では、ゲート電極中の不純物の拡散バリアー層( $Si_3N_4$ 膜)43を形成した後にゲート電極41に不純物を導入しているため、ゲート電極中の不純物の外方拡散や横方向の空間的な再分布の問題は生じない。即ち図32(b)に示すような工程の場合である。

・【0080】したがって、ゲート電極41へイオン注入するイオン種およびそのDose量により、正確に狙いとする仕事関数を有する高融点金属シリサイドゲート電極を得ることが可能となる。特に、WSixゲート電極中の不純物の横方向の相互拡散の影響をなくすることができるため、Wafer面内で異なるイオン種やDose量を導入して、異なる仕事関数を有するゲート電極を作製する場合に相互の影響を受けずに正確に仕事関数を制御することが可能となる。

・【0081】また、ゲート電極の不純物の外方拡散を抑制する薄膜(拡散バリアー層)の形成方法や形成条件(特に熱処理プロセス)によらず、正確に制御された目的とする不純物濃度を有する高融点金属シリサイドゲート電極を得ることが可能となる。

・【0082】尚、上記第3の実施の形態では、Bulk Si基板上に形成され仕事関数が制御されたWSixゲート電極41を有するMOS型半導体装置の製造に本発明を適用しているが、他のゲート電極を有する半導体装置の製造に本発明を適用することも可能であり、例えばMoSixのような高融点金属シリサイドからなるゲート電極を有する半導体装置の製造に本発明を適用することも可能である。このMoSixのように $\sim 1 \times 10^{13} \text{cm}^{-2}$ の低いDose量からその仕事関数が大きく変化するようなシリサイドを用いてゲート電極を形成する場合に、本発明は特に有効である。すなわち、拡散防止層( $Si_3N_4$ 膜)を形成する前に、 $V_{th}$ が異なるTrを作製するべく場所によって異なる不純物の種類、異なる不純物

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濃度等のイオンをゲート電極に打ち分けている場合に、ゲート電極中の不純物の外方拡散や横方向の空間的な再分布が大きな問題となる。それは、例えばLP-CVDによる $Si_3N_4$ 膜を形成する時のAuto-Dopingにより、気相を通じて不純物濃度の空間的な再分布等が生じて、これによりゲート電極の仕事関数が狙いとする値から変動する結果、出来上りのTrの $V_{th}$ も狙いとするものからはずれてしまうからである。しかし、第3の実施の形態のように拡散防止層( $Si_3N_4$ 膜43)を形成した後に、ゲート電極41に不純物を導入すれば、拡散防止層の形成時の熱プロセスの影響を受けることがない。

・【0083】また、Bulk Si基板1上に形成される半導体装置に本発明を適用しているが、SOI基板上に形成される半導体装置に本発明を適用することも可能である。

・【0084】また、ゲート電極41に接する膜であってゲート電極41中の不純物の外方拡散を抑制する $Si_3N_4$ 膜53aをLP-CVD法により堆積させているが、ゲート電極41自身を直接窒化して高融点金属窒化膜(WNx膜)を成長させることも可能である。

・【0085】また、上記第3の実施の形態中で用いた各薄膜の膜厚等のパラメータは、全てその一例であって、目的とする半導体装置によっていずれのパラメータも適宜設計変更が可能である。

・【0086】図23～図30は、本発明の第4の実施の形態による半導体装置の製造方法を示す断面図であり、この実施の形態は、ゲート電極の高融点金属シリサイドを加工した後で不純物の外方拡散防止用の薄膜を堆積し、この薄膜を通してゲート電極にイオン注入を行う場合について説明する。

・【0087】先ず、図23に示すように、シリコン基板1にはLOCOS酸化膜2及び図示せぬWellが設けられ、このLOCOS酸化膜2及びWell等を用いて素子分離が行われる。次に、素子領域のシリコン基板1の表面上には熱酸化法によりゲート酸化膜3が形成(成長)される。

・【0088】この後、図24に示すように、ゲート酸化膜3及びLOCOS酸化膜2の上にはゲート電極となる厚さが例えば $\sim 100 \text{nm}$ 程度のWSix膜41が堆積される。この時のWSix膜41の堆積条件は、第3の実施の形態で示したものと同様である。WSix膜41の組成比は $W:Si=1:3.0$ である。

・【0089】ここでWSix膜41は、化学量論組成比よりもSi Richとなっている。これは、後の工程でWSix膜41に導入されるAsやBもしくはPhosのような不純物の種類及びそのDose量に応じて、出来上りのゲート電極の仕事関数が制御される様にするためである。

・【0090】次に、図25に示すように、WSix膜4

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1 の上にはフォトレジスト膜 67 が形成され、このフォトレジスト膜 67 はゲート電極のパターンを有するものである。

・【0091】この後、図 26 に示すように、このフォトレジスト膜 67 をマスクとして  $WSi_x$  膜 41 がエッチング加工される。次に、フォトレジスト膜 67 が除去される。

・【0092】次に、図 27 に示すように、 $WSi_x$  ゲート電極 41 及びシリコン基板 1 の上には  $LP-CVD$  法により厚さが例えば  $\sim 10nm$  程度の  $Si_3N_4$  膜 43 が堆積される。この時の  $Si_3N_4$  膜 43 の堆積条件は、第 3 の実施の形態で示したものと同様である。この  $Si_3N_4$  膜 43 はゲート電極 41 からの不純物の外方拡散を抑制するための膜である。

・【0093】次に、シリコン基板 1 における図示せぬ  $LDD$  領域に不純物を導入することにより、シリコン基板 1 には図示せぬ  $LDD$  層が形成される。尚、この不純物の導入は、 $N-MOSTr$  の場合と  $P-MOSTr$  の場合とで、レジストマスクを用いて適宜イオンを打ち分ける。

・【0094】この後、図 28 に示すように、全面には  $SiO_2$  膜 69 が堆積される。次に、この  $SiO_2$  膜 69 を異方性加工を用いた  $Etch Back$  することにより、ゲート電極 41 の側壁には  $Si_3N_4$  43 を介して  $SiO_2$  からなる  $LDD\ Spacer$  69 が形成される。この時の  $SiO_2$  膜 69 の堆積条件および加工条件は共に第 3 の実施の形態で示したものと同様である。

・【0095】次に、図 29 に示すように、チャネリング防止用の薄い酸化膜 55 をシリコン基板 1 上に堆積した後、シリコン基板 1 の上にはフォトレジスト膜 57 が形成される。このフォトレジスト膜 57 のパターン形状はソース・ドレイン領域形成部を開口したものである。この後、このフォトレジスト膜 57 をマスクとしてゲート電極 41 及びシリコン基板 1 のソース・ドレイン領域の拡散層への不純物の導入（イオン注入）を行う。尚、このイオン注入は、 $N-MOSTr$  の場合と  $P-MOSTr$  の場合とでレジストマスクを用いて適宜打ち分ける。

・【0096】次に、フォトレジスト膜 57 を除去した後、ゲート電極 41、 $LDD$  層、ソース・ドレイン領域の拡散層、その他の不純物導入層を活性化させるための熱処理が行われる。この時の熱処理条件は、例えば  $Ar$  雰囲気中で温度を  $1000^{\circ}C$ 、処理時間を 10 秒とし、 $RTA$  処理を用いる。

・【0097】この後、図 30 に示すように、通常のプロセスにて、 $Si_3N_4$  膜 43、 $Side\ all\ Spacer$  69、シリコン基板 1 の上には層間絶縁膜 61 が堆積される。次に、この層間絶縁膜 61 にはコンタクトホール 61a が設けられ、このコンタクトホール 61a 内はメタル 63 により穴埋めされ、このメタル 63 の上には配線 65 が形成され、素子を完成させる。

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・【0098】上記第 4 の実施の形態によれば、図 26 に示す工程で  $WSi_x$  膜 41 をパターンニングしてゲート電極を形成した後に、図 27 に示す工程でゲート電極 41 上に拡散バリアー層としての  $Si_3N_4$  膜 43 を形成し、その後の図 29 の工程でゲート電極 41 に不純物をイオン注入等により導入している。これにより、1 つの単体  $Tr$  でゲート電極の仕事関数は不純物濃度に応じて決まり、ゲート電極中の不純物の横方向の相互拡散による仕事関数の変動は生じない。

・【0099】つまり、ゲート電極（高融点金属シリサイド膜）の加工の後に該ゲート電極に不純物をイオン注入により導入し、その後、該ゲート電極に不純物拡散防止膜を形成する場合には、この不純物拡散防止膜の形成時の熱により、ゲート電極中の不純物の外方拡散等の問題が生じる。即ち図 32 (c) に示すような工程の場合である。しかし、第 4 の実施の形態では、高融点金属シリサイド膜に不純物のイオン注入を行う前に、不純物拡散防止膜を形成しているため、ゲート電極中の不純物の外方拡散や横方向の空間的な再分布の問題は生じない。即ち図 32 (d) に示すような工程の場合である。したがって、上記第 4 の実施の形態においても第 3 の実施の形態と同様の効果を得ることができる。

・【0100】また、図 29 に示す工程でゲート電極 41 及びソース・ドレイン領域の拡散層への不純物の導入を行うため、拡散層に導入されるイオン種とゲート電極に導入されるイオン種とが同じものになる。その結果、プロセス設計上の自由度は幾らか失われてしまうが、第 3 の実施の形態に比べてプロセスを非常に簡略化できるため、半導体装置の製造コストを下げることができる。

・【0101】尚、上記第 4 の実施の形態では、 $Bulk\ Si$  基板上に形成され仕事関数が制御された  $WSi_x$  ゲート電極 41 を有する  $MOS$  型半導体装置の製造に本発明を適用しているが、他のゲート電極を有する半導体装置の製造に本発明を適用することも可能であり、例えば  $Mosix$  のような高融点金属シリサイドからなるゲート電極を有する半導体装置の製造に本発明を適用することも可能である。

・【0102】また、 $Bulk\ Si$  基板 1 上に形成される半導体装置に本発明を適用しているが、 $SOI$  基板上に形成される半導体装置に本発明を適用することも可能である。

・【0103】また、ゲート電極 41 に接する膜であってゲート電極 41 中の不純物の外方拡散を抑制する  $Si_3N_4$  膜 43 を  $LP-CVD$  法により堆積させているが、ゲート電極 41 自身を直接窒化して高融点金属窒化膜 ( $WNx$  膜) を成長させることも可能である。

・【0104】また、上記第 3 の実施の形態中で用いた各薄膜の膜厚等のパラメータは、全てその一例であって、目的とする半導体装置によっていずれのパラメータも適宜設計変更が可能である。

・【0105】

・【発明の効果】以上説明したように請求項1～13に係る発明によれば、高濃度の不純物を導入したゲート電極の上部及び側壁部に窒素を含む絶縁膜を形成している。したがって、ゲート電極を形成した後の製造工程に熱プロセスがある場合でも、その熱プロセスによって生じる出来上がりのゲート電極の仕事関数の変動を抑えてしきい値電圧のバラツキを小さくすることができる。

・【0106】また、請求項14に係る発明によれば、高融点金属シリサイド膜上に不純物の外方拡散防止用の薄膜を形成した後に、この薄膜を通して高融点金属シリサイド膜に不純物を導入している。また、請求項15に係る発明によれば、高融点金属シリサイド膜をパターンニングした後に、ゲート電極表面の全部又は一部に不純物の外方拡散防止用の薄膜を形成し、その後、この薄膜を通して該ゲート電極に不純物を導入している。したがって、ゲート電極中の不純物の外方拡散を抑制するために比較的高温にて拡散バリアー層を形成するプロセスにおいても、ゲート電極の不純物濃度を狙いとする値に正確に制御できる。

・【図面の簡単な説明】

・【図1】図1(a)は、この発明の第1の実施の形態による半導体装置を示す断面図であり、図1(b)は、図1(a)に示す第1の実施の形態による半導体装置の変形例を示す半導体装置の断面図である。

・【図2】この発明の第2の実施の形態による半導体装置の製造方法を示す断面図である。

・【図3】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図2の次の工程を示す断面図である。

・【図4】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図3の次の工程を示す断面図である。

・【図5】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図4の次の工程を示す断面図である。

・【図6】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図5の次の工程を示す断面図である。

・【図7】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図6の次の工程を示す断面図である。

・【図8】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図7の次の工程を示す断面図である。

・【図9】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図8の次の工程を示す断面図である。

・【図10】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図9の次の工程を示す

断面図である。

・【図11】この発明の第2の実施の形態による半導体装置の製造方法を示すものであり、図10の次の工程を示す断面図である。

・【図12】本発明の第3の実施の形態による半導体装置の製造方法を示す断面図である。

・【図13】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図12の次の工程を示す断面図である。

・【図14】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図13の次の工程を示す断面図である。

・【図15】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図14の次の工程を示す断面図である。

・【図16】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図15の次の工程を示す断面図である。

・【図17】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図16の次の工程を示す断面図である。

・【図18】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図17の次の工程を示す断面図である。

・【図19】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図18の次の工程を示す断面図である。

・【図20】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図19の次の工程を示す断面図である。

・【図21】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図20の次の工程を示す断面図である。

・【図22】本発明の第3の実施の形態による半導体装置の製造方法を示すものであり、図21の次の工程を示す断面図である。

・【図23】本発明の第4の実施の形態による半導体装置の製造方法を示す断面図である。

・【図24】本発明の第4の実施の形態による半導体装置の製造方法を示すものであり、図23の次の工程を示す断面図である。

・【図25】本発明の第4の実施の形態による半導体装置の製造方法を示すものであり、図24の次の工程を示す断面図である。

・【図26】本発明の第4の実施の形態による半導体装置の製造方法を示すものであり、図25の次の工程を示す断面図である。

・【図27】本発明の第4の実施の形態による半導体装置の製造方法を示すものであり、図26の次の工程を示す断面図である。

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・【図28】本発明の第4の実施の形態による半導体装置の製造方法を示すものであり、図27の次の工程を示す断面図である。

・【図29】本発明の第4の実施の形態による半導体装置の製造方法を示すものであり、図28の次の工程を示す断面図である。

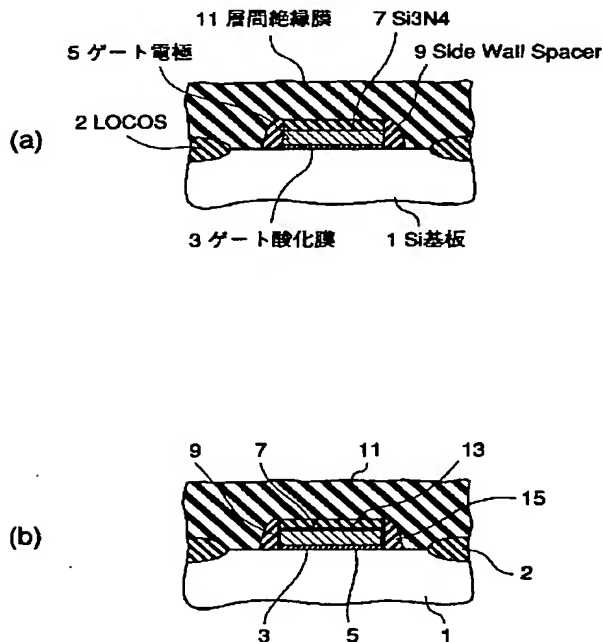
・【図30】本発明の第4の実施の形態による半導体装置の製造方法を示すものであり、図29の次の工程を示す断面図である。

・【図31】図31(a)は、面内でイオン種、Dose量を $T_r$ の狙いとする $V_{th}$ により打ち分けて $WSi_x$ 膜にイオン注入をした後の状態を示す断面図であり、図31(b)は、図31(a)に示す $WSi_x$ 膜の上に不純物の拡散防止層を形成した後の状態であって、気相を通したAuto-Dopingや $WSi_x$ の横方向拡散により、不純物の再分布が生じている状態を示す断面図である。

・【図32】図32(a)、(b)は、ゲート電極の加工前に不純物を注入する製造方法を示す図であり、図32(c)、(d)は、ゲート電極の加工後に不純物を注入する製造方法を示す図である。

・【図33】図33(a)は、従来の半導体装置を示す断面図であり、図33(b)は、図33(a)に示す半導体装置におけるゲート電極及びその近傍部分(Aの領

・【図1】



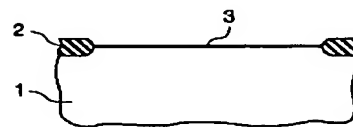
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\*域)を示す拡大断面図である。

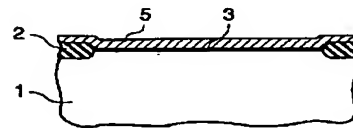
・【符号の説明】

1…Bulk シリコン基板(半導体基板)、2…LOCOS酸化膜、3…ゲート酸化膜、5…ゲート電極、7… $Si_3N_4$ 膜、9…Side Wall Spacer ( $Si_3N_4$ 膜)、11…層間絶縁膜、11a…コンタクトホール、13、15… $SiO_2$ 膜、21…フォトリソ膜、23… $BF_3$ のイオン注入、25、27…フォトリソ膜、29… $BF_3$ のイオン注入、31…メタル、33…配線、41… $WSi_x$ 膜、43… $Si_3N_4$ 膜、45…フォトリソ膜、47… $B^+$  Ion、49… $SiO_2$ 膜、51…フォトリソ膜、53…LDD Spacer ( $SiO_2/Si_3N_4$  Side Wall Spacer)、53a… $Si_3N_4$ 膜、53b… $SiO_2$ 膜、55…チャネリング防止用の薄い酸化膜、57…フォトリソ膜、59… $BF_3$ イオン、61…層間絶縁膜、61a…コンタクトホール、63…メタル、65…配線、67…フォトリソ膜、69… $SiO_2$ 膜、101…シリコン基板、102…ゲート酸化膜1、103…LOCOS酸化膜、105…ゲート電極、107…層間絶縁膜( $SiO_2$ )、111…Bの析出、113…Bの層間絶縁膜への拡散。

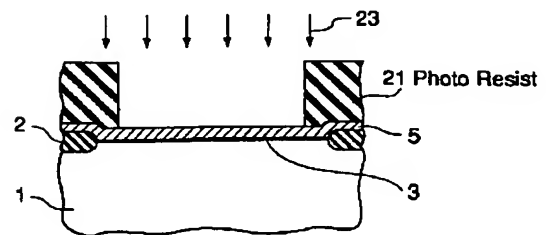
・【図2】



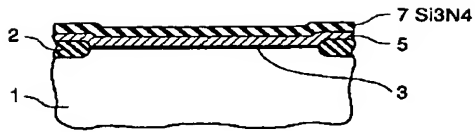
・【図3】



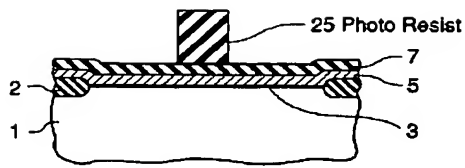
・【図4】



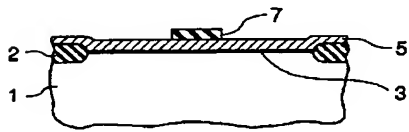
・【図5】



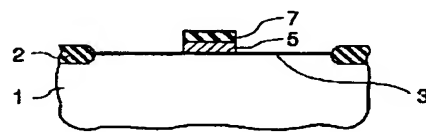
・【図6】



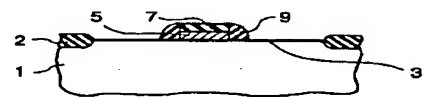
・【図7】



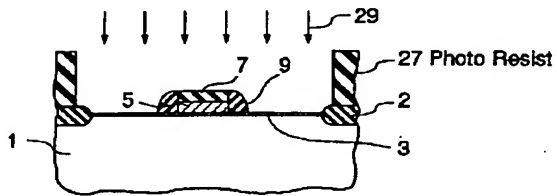
・【図8】



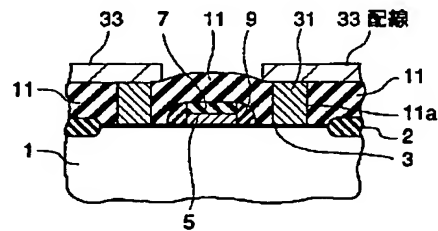
・【図9】



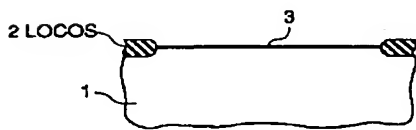
・【図10】



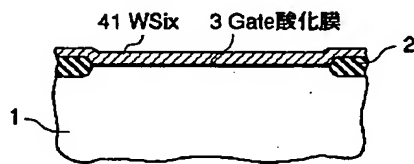
・【図11】



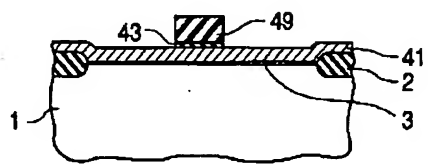
・【図12】



・【図13】



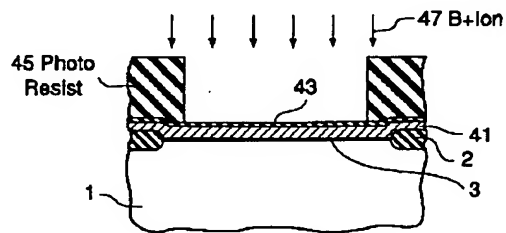
・【図18】



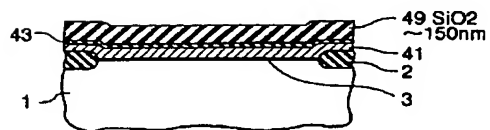
・【図14】



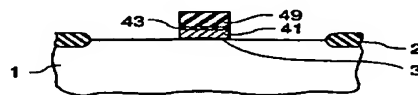
・【図15】



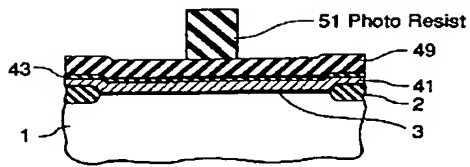
・【図16】



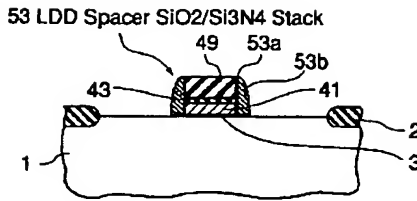
・【図19】



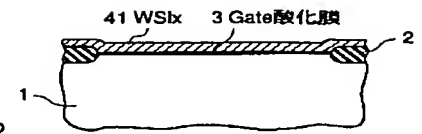
・【図17】



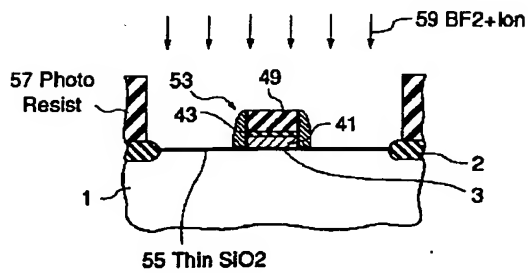
・【図20】



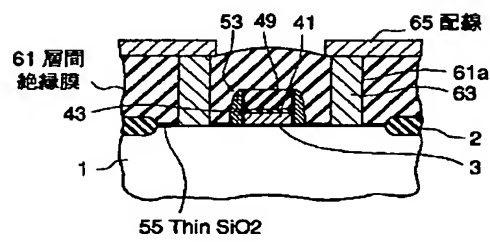
・【図24】



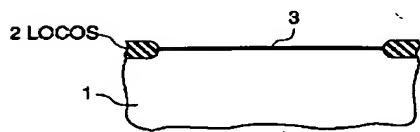
・【図21】



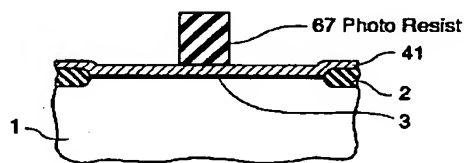
・【図22】



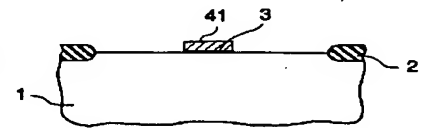
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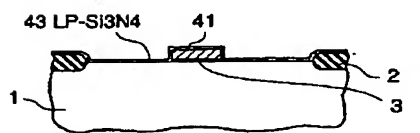
・【図25】



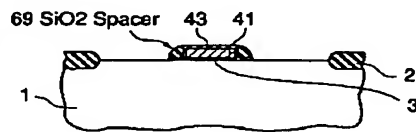
・【図26】



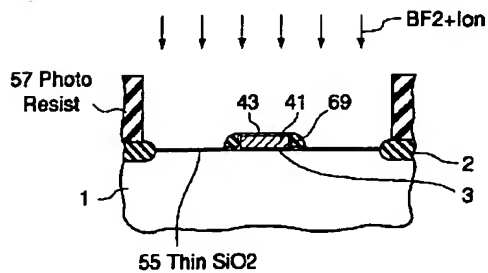
・【図27】



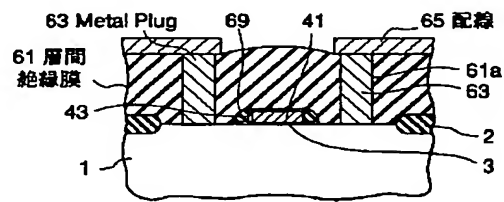
・【図28】



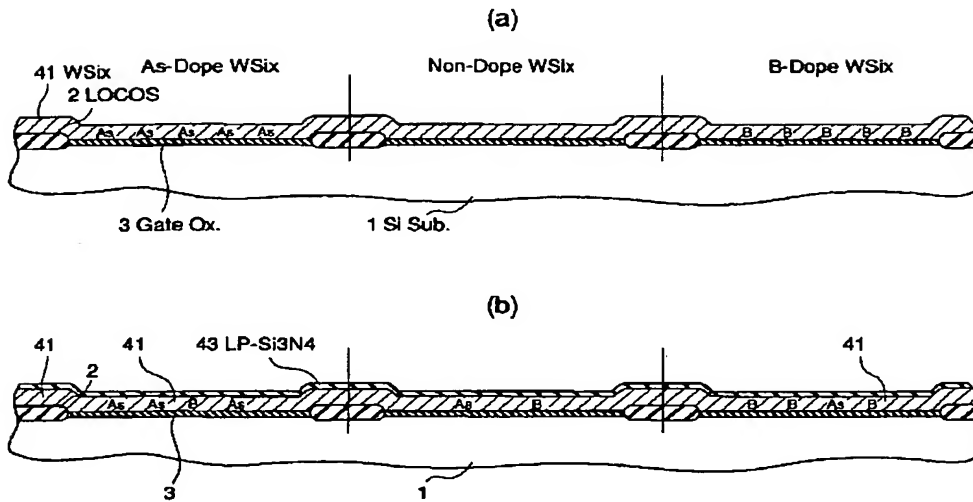
・【図29】



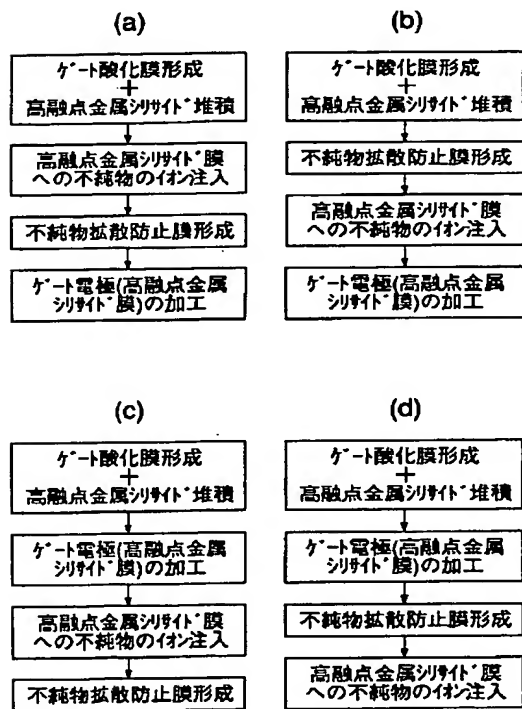
・【図30】



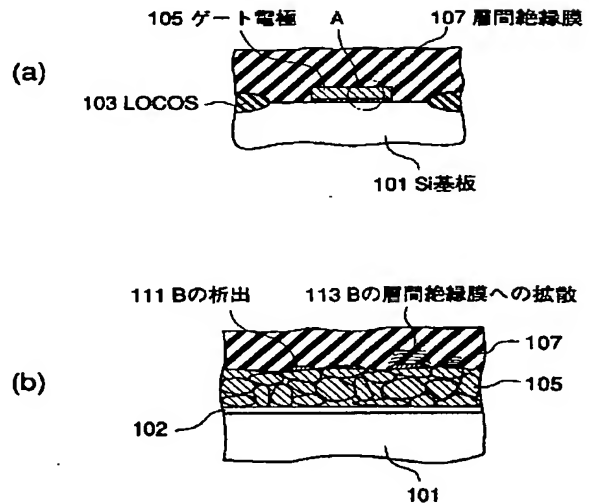
・【図 3 1】



・【図 3 2】



・【図 3 3】



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